

Datasheet

APM32F030xC

Arm[®] Cortex[®] -M0+ based 32-bit MCU

Version: V1.5

1 Product characteristics

■ Core

- 32-bit Arm® Cortex® -M0+ core
- Up to 48MHz working frequency

■ On-chip memory

- Flash: 256KB
- SRAM: 32KB

■ Clock

- HSECLK: 4~32MHz external crystal/ceramic oscillator supported
- LSECLK: 32.768KHz crystal/ceramic oscillator supported
- HSICLK: 8MHz RC oscillator calibrated by factory
- HSICLK14: 14MHz RC oscillator supported
- LSICLK: 40KHz RC oscillator supported
- PLL: Phase locked loop, 2~16 times of frequency supported

■ Reset and power management

- V_{DD} range: 2.0~3.6V
- V_{DDA} range: V_{DD} ~3.6V
- Power-on/power-down reset (POR/PDR) supported

■ Low-power mode

- Sleep, stop and standby modes supported

■ DMA

- 5-channel DMA controller

■ Debugging interface

- SWD

■ I/O

- Up to 51 I/Os
- All I/Os can be mapped to external interrupt vector

- Up to 29 FT I/Os

■ Communication peripherals

- 2 I2C interfaces (1Mbit/s), all of which support SMBus/PMBus
- 6 USARTs, support synchronous transmission function
- 2 SPI (18Mbit/s) interfaces

■ Analog peripherals

- 1 12-bit ADC, support up to 16 external channels

■ Timer

- 1 16-bit advanced timer TMR1 that can provide 7-channel PWM output, support dead zone generation and braking input functions
- 5 16-bit general-purpose timers TMR3/14/15/16 and TMR17, with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions.
- 2 16-bit basic timers TMR6/7
- 2 watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
- 1 24-bit autodecrement SysTick Timer

■ RTC

- Support calendar function
- Alarm and periodic wake-up from stop/standby mode

■ CRC computing unit

■ 96-bit unique device ID (UID)

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2 Product information

See the following table for APM32F030xC product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32F030xC Series Chips

Product		APM32F030	
Model		CCTx	RCTx
Package		LQFP48	LQFP64
Core and maximum working frequency		Arm® 32-bit Cortex®-M0+@48MHz	
Operating voltage		2.0~3.6V	
Flash(KB)		256	
SRAM(KB)		32	
GPIOs		37	51
Communication interface	USART	6	
	SPI	2	
	I2C	2	
Timer	16-bit advanced	1	
	16-bit general	5	
	16-bit basic	2	
	System tick timer	1	
	Watchdog	2	
Real-time clock		1	
12-bit ADC	Unit	1	
	External channel	10	16
	Internal channel	2	
Operating temperature		Ambient temperature: -40°C to 85°C/-40°C to 105°C Junction temperature: -40°C to 105°C/-40°C to 125°C	

Note:

- (1) When x is 6, ambient temperature is: from -40°C to 85°C, and the junction temperature is from -40°C to 105°C.
- (2) When x is 7, ambient temperature is: from -40°C to 105°C, and the junction temperature is from -40°C to 125°C.

3 Pin information

3.1 Pin distribution

Figure 1 Distribution Diagram of APM32F030xCTx Series LQFP64 Pins

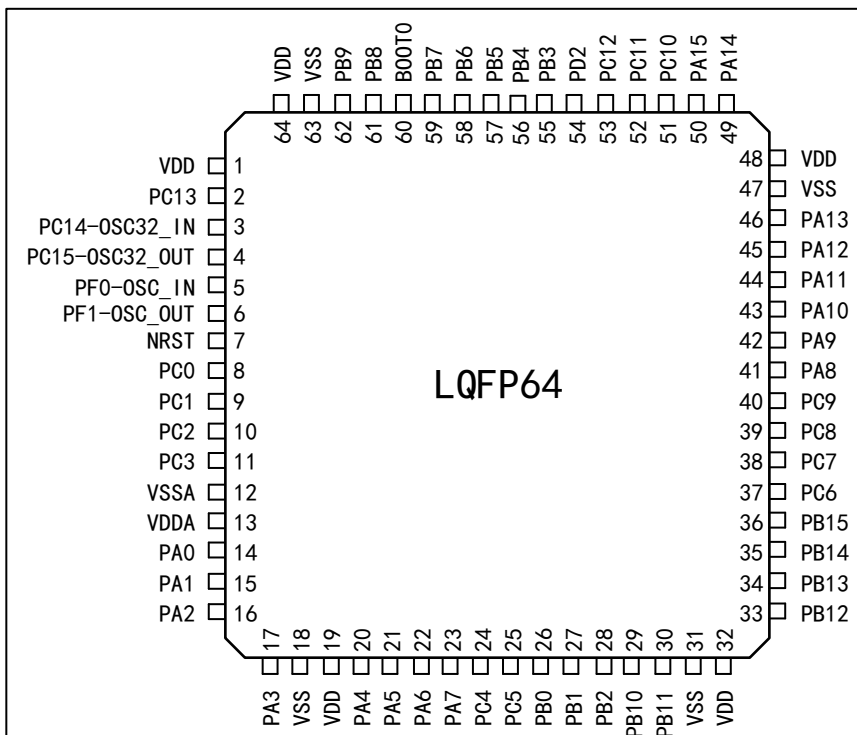
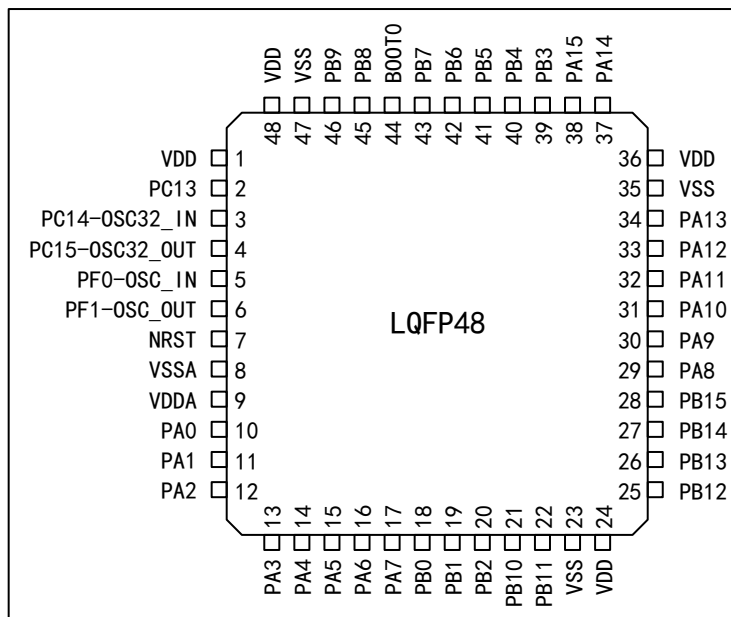


Figure 2 Distribution Diagram of APM32F030xCTx Series LQFP48 Pins



3.2 Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name		Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name
Pin type	P	Power pin
	I	Only input pin
	I/O	I/O pin
I/O structure	5T	FT I/O
	5Tf	FT I/O, FM + function
	STDA	I/O with 3.3V standard, directly connected to ADC
	STD	I/O with 3.3 V tolerance
	B	Dedicated Boot0 pin
	RST	Bidirectional reset pin with built-in pull-up resistor
Note		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset
Pin function	Default multiplexing function	Function directly selected/enabled through peripheral register
	Additional function	Function selected through GPIO multiplexing function register

Table 3 Description of APM32F030xCTx by Pin Number

Name (Function after reset)	Type	Structure	Default multiplexing function	Additional function	LQFP48	LQFP64
VDD	P	-	Digital power supply		1	1
PC13	I/O	STD	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2	2	2
PC14-OSC32_IN (PC14)	I/O	STD	-	OSC32_IN	3	3
PC15-OSC32_OUT (PC15)	I/O	STD	-	OSC32_OUT	4	4
PF0-OSC_IN (PF0)	I/O	STD	I2C1_SDA	OSC_IN	5	5
PF1-OSC_OUT (PF1)	I/O	STD	I2C1_SCL	OSC_OUT	6	6
NRST	I/O	RST	Chip reset input/internal reset output (active low)		7	7

Name (Function after reset)	Type	Structure	Default multiplexing function	Additional function	LQFP48	LQFP64
PC0	I/O	STDA	EVENTOUT, USART6_TX	ADC_IN10	-	8
PC1	I/O	STDA	EVENTOUT, USART6_RX	ADC_IN11	-	9
PC2	I/O	STDA	SPI2_MISO, EVENTOUT	ADC_IN12	-	10
PC3	I/O	STDA	SPI2_MOSI, EVENTOUT	ADC_IN13	-	11
VSSA	P	-	Analog ground		8	12
VDDA	P	-	Analog power supply		9	13
PA0	I/O	STDA	USART2_CTS, USART4_TX	ADC_IN0, RTC_TAMP2, WKUP1	10	14
PA1	I/O	STDA	USART2_RTS, EVENTOUT, USART4_RX	ADC_IN1	11	15
PA2	I/O	STDA	USART2_TX, TMR15_CH1	ADC_IN2, WKUP4	12	16
PA3	I/O	STDA	USART2_RX, TMR15_CH2	ADC_IN3	13	17
VSS	P	-	Ground		-	18
VDD	P	-	Digital power supply		-	19
PA4	I/O	STDA	SPI1_NSS, USART2_CK, TMR14_CH1, USART6_TX	ADC_IN4	14	20
PA5	I/O	STDA	SPI1_SCK, USART6_RX	ADC_IN5	15	21
PA6	I/O	STDA	SPI1_MISO, TMR3_CH1, TMR1_BKIN, TMR16_CH1, EVENTOUT, USART3_CTS	ADC_IN6	16	22
PA7	I/O	STDA	SPI1_MOSI, TMR3_CH2, TMR14_CH1, TMR1_CH1N, TMR17_CH1, EVENTOUT	ADC_IN7	17	23

Name (Function after reset)	Type	Structure	Default multiplexing function	Additional function	LQFP48	LQFP64
PC4	I/O	STDA	EVENTOUT, USART3_TX	ADC_IN14	-	24
PC5	I/O	STDA	USART3_RX	ADC_IN15, WKUP5	-	25
PB0	I/O	STDA	TMR3_CH3, TMR1_CH2N, EVENTOUT, USART3_CK	ADC_IN8	18	26
PB1	I/O	STDA	TMR3_CH4, TMR14_CH1, TMR1_CH3N, USART3_RTS	ADC_IN9	19	27
PB2	I/O	5T	-	-	20	28
PB10	I/O	5T	SPI2_SCK, I2C2_SCL, USART3_TX	-	21	29
PB11	I/O	5T	I2C2_SDA, EVENTOUT, USART3_RX	-	22	30
VSS	P	-	Ground		23	31
VDD	P	-	Digital power supply		24	32
PB12	I/O	5T	SPI2_NSS, TMR1_BKIN, EVENTOUT, USART3_CK	-	25	33
PB13	I/O	5T	SPI2_SCK, I2C2_SCL, TMR1_CH1N, USART3_CTS	-	26	34
PB14	I/O	5T	SPI2_MISO, I2C2_SDA, TMR1_CH2N, TMR15_CH1, USART3_RTS	-	27	35
PB15	I/O	5T	SPI2_MOSI, TMR1_CH3N, TMR15_CH1N, TMR15_CH2	RTC_REFIN, WKUP7	28	36
PC6	I/O	5T	TMR3_CH1	-	-	37
PC7	I/O	5T	TMR3_CH2	-	-	38

Name (Function after reset)	Type	Structure	Default multiplexing function	Additional function	LQFP48	LQFP64
PC8	I/O	5T	TMR3_CH3	-	-	39
PC9	I/O	5T	TMR3_CH4	-	-	40
PA8	I/O	5T	USART1_CK, TMR1_CH1, EVENTOUT, MCO	-	29	41
PA9	I/O	5T	USART1_TX, TMR1_CH2, TMR15_BKIN, I2C1_SCL	-	30	42
PA10	I/O	5T	USART1_RX, TMR1_CH3, TMR17_BKIN, I2C1_SDA	-	31	43
PA11	I/O	5T	USART1_CTS, TMR1_CH4, EVENTOUT, I2C2_SCL	-	32	44
PA12	I/O	5T	USART1_RTS, TMR1_ETR, EVENTOUT, I2C2_SDA	-	33	45
PA13 (SWDIO)	I/O	5T	IR_OUT,SWDIO	-	34	46
VSS	P	-	Ground		35	47
VDD	P	-	Digital power supply		36	48
PA14 (SWCLK)	I/O	5T	USART2_TX, SWCLK	-	37	49
PA15	I/O	5T	SPI1_NSS, USART2_RX, USART4_RTS, EVENTOUT	-	38	50
PC10	I/O	5T	USART3_TX, USART4_TX	-	-	51
PC11	I/O	5T	USART3_RX, USART4_RX	-	-	52
PC12	I/O	5T	USART3_CK, USART4_CK, USART5_TX	-	-	53

Name (Function after reset)	Type	Structure	Default multiplexing function	Additional function	LQFP48	LQFP64
PD2	I/O	5T	TMR3_ETR, USART3_RTS, USART5_RX	-	-	54
PB3	I/O	5T	SPI1_SCK, EVENTOUT, USART5_TX	-	39	55
PB4	I/O	5T	SPI1_MISO, TMR3_CH1, EVENTOUT, TMR17_BKIN, USART5_RX	-	40	56
PB5	I/O	STD	SPI1_MOSI, I2C1_SMBA, TMR16_BKIN, TMR3_CH2, USART5_CK_RTS	WKUP6	41	57
PB6	I/O	5Tf	I2C1_SCL, USART1_TX, TMR16_CH1N	-	42	58
PB7	I/O	5Tf	I2C1_SDA, USART1_RX, TMR17_CH1N, USART4_CTS	-	43	59
BOOT0	I	B	Startup selection		44	60
PB8	I/O	5T	I2C1_SCL, TMR16_CH1	-	45	61
PB9	I/O	5T	I2C1_SDA, IR_OUT, SPI2_NSS, TMR17_CH1, EVENTOUT	-	46	62
VSS	P	-	Ground		47	63
VDD	P	-	Digital power supply		48	64

Note:

- (1) PC13, PC14 and PC15 are powered through power switch. Since the switch only sinks limited current (3mA), the use of GPIO from PC13 to PC15 in output mode is limited: the speed shall not exceed 2MHz when the heavy load is 30pF; not used for current source (e.g. driving LED).
- (2) After reset, PA13 and PA14 are configured as SWDIO and SWCLK multiplexing functions, and the internal pull-up of SWDIO pin and the internal pull-down of SWCLK pin are activated.

Table 4 Port A Multiplexing Function Configuration

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA0	-	USART2_CTS	-	-	USART4_TX	-	-
PA1	EVENTOUT	USART2_RTS	-	-	USART4_RX	TMR15_CH1N	-
PA2	TMR15_CH1	USART2_TX	-	-	-	-	-
PA3	TMR15_CH2	USART2_RX	-	-	-	-	-
PA4	SPI1_NSS	USART2_CK	-	-	TMR14_CH1	USART6_TX	-
PA5	SPI1_SCK	-	-	-	-	USART6_RX	-
PA6	SPI1_MISO	TMR3_CH1	TMR1_BKIN	-	USART3_CTS	TMR16_CH1	EVENTOUT
PA7	SPI1_MOSI	TMR3_CH2	TMR1_CH1N	-	TMR14_CH1	TMR17_CH1	EVENTOUT
PA8	MCO	USART1_CK	TMR1_CH1	EVENTOUT	-	-	-
PA9	TMR15_BKIN	USART1_TX	TMR1_CH2	-	I2C1_SCL	MCO	-
PA10	TMR17_BKIN	USART1_RX	TMR1_CH3	-	I2C1_SDA	-	-
PA11	EVENTOUT	USART1_CTS	TMR1_CH4	-	-	SCL	-
PA12	EVENTOUT	USART1_RTS	TMR1_ETR	-	-	SDA	-
PA13	SWDIO	IR_OUT	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-
PA15	SPI1_NSS	USART2_RX	-	EVENTOUT	USART4_RTS	-	-

Table 5 Port B Multiplexing Function Configuration

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TMR3_CH3	TMR1_CH2N	-	USART3_CK	-
PB1	TMR14_CH1	TMR3_CH4	TMR1_CH3N	-	USART3_RTS	-
PB2	-	-	-	-	-	-
PB3	SPI1_SCK	EVENTOUT	-	-	USART5_TX	-
PB4	SPI1_MISO	TMR3_CH1	EVENTOUT	-	USART5_RX	TMR17_BKIN
PB5	SPI1_MOSI	TMR3_CH2	TMR16_BKIN	I2C1_SMBA	USART5_CK_RTS	-
PB6	USART1_TX	I2C1_SCL	TMR16_CH1N	-	-	-
PB7	USART1_RX	I2C1_SDA	TMR17_CH1N	-	USART4_CTS	-
PB8	-	I2C1_SCL	TMR16_CH1	-	-	-
PB9	IR_OUT	I2C1_SDA	TMR17_CH1	EVENTOUT	-	SPI2_NSS
PB10	-	I2C2_SCL	-	-	USART3_TX	SPI2_SCK
PB11	EVENTOUT	I2C2_SDA	-	-	USART3_RX	-
PB12	SPI2_NSS	EVENTOUT	TMR1_BKIN	-	USART3_RTS	TMR15
PB13	SPI2_SCK	-	TMR1_CH1N	-	USART3_CTS	I2C2_SCL

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB14	SPI2_MISO	TMR15_CH1	TMR1_CH2N	-	USART3_RTS	I2C2_SDA
PB15	SPI2_MOSI	TMR15_CH2	TMR1_CH3N	TMR15_CH1N	-	-

Table 6 Port C Multiplexing Function Configuration

Pin name	AF0	AF1	AF2
PC0	EVENTOUT	-	USART6_TX
PC1	EVENTOUT	-	USART6_RX
PC2	EVENTOUT	SPI2_MISO	-
PC3	EVENTOUT	SPI2_MOSI	-
PC4	EVENTOUT	USART3_TX	-
PC5	-	USART3_RX	-
PC6	TMR3_CH1	-	-
PC7	TMR3_CH2	-	-
PC8	TMR3_CH3	-	-
PC9	TMR3_CH4	-	-
PC10	USART4_TX	USART3_TX	-
PC11	USART4_RX	USART3_RX	-
PC12	USART4_CK	USART3_CK	USART5_TX
PC13	-	-	-
PC14	-	-	-
PC15	-	-	-

Table 7 Port D Multiplexing Function Configuration

Pin name	AF0	AF1	AF2
PD2	TMR3_ETR	USART3_RTS	USART5_RX

Table 8 Port F Multiplexing Function Configuration

Pin name	AF0	AF1
PF0	-	I2C1_SDA
PF1	-	I2C1_SCL

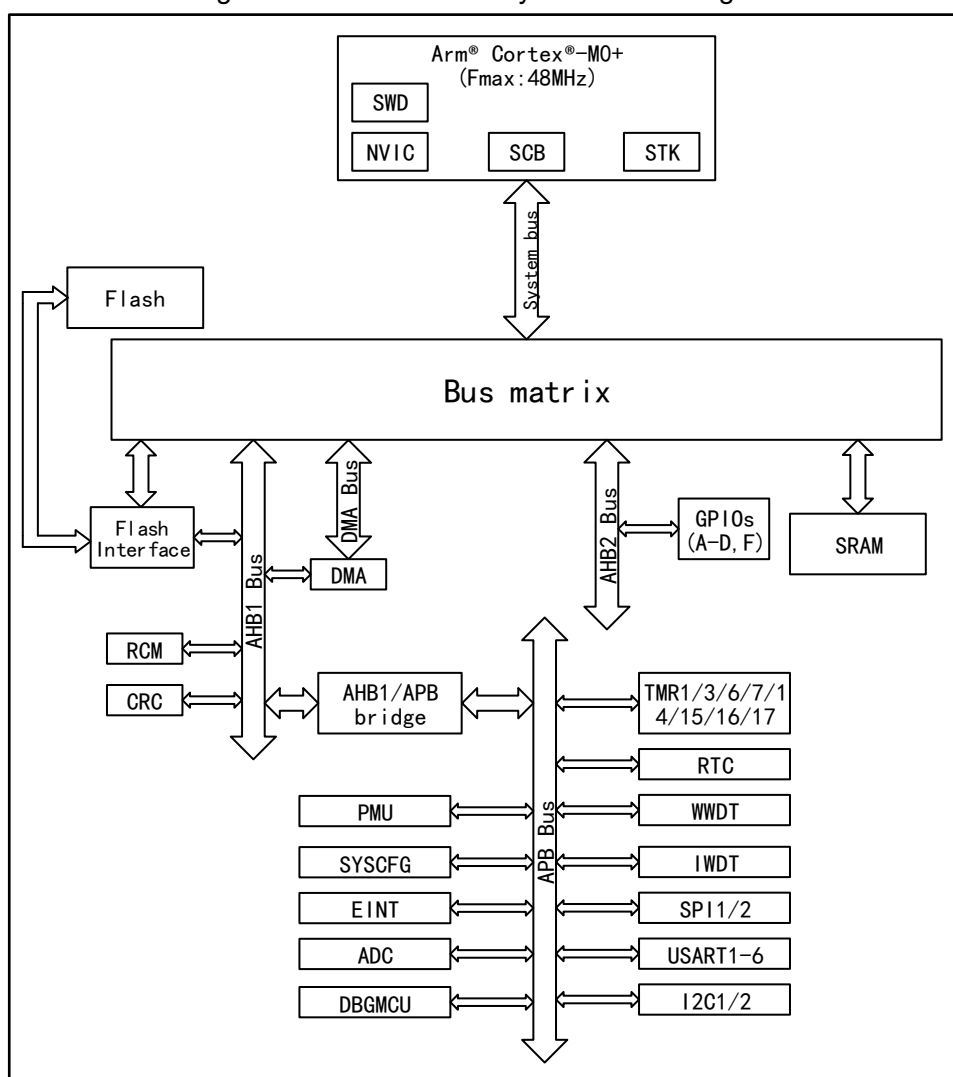
4 Functional description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32F030xC series products; for information about the Arm® Cortex®-M0+ core, please refer to the Arm® Cortex®-M0+ technical reference manual, which can be downloaded from Arm’s website.

4.1 System architecture

4.1.1 System Block Diagram

Figure 3 APM32F030xC System Block Diagram



4.1.2 Memory mapping

Table 9 APM32F030xC Storage Mapping Table

Region	Start address	Peripheral Name
Code	0x0000 0000	Code mapping area
Code	0x0004 0000	Reserved

Region	Start address	Peripheral Name
Code	0x0800 0000	Main memory area
Code	0x0804 0000	Reserved
Code	0x1FFF D800	System memory
Code	0x1FFF F800	Option byte
Code	0x1FFF FC00	Reserved
SRAM	0x2000 0000	SRAM
—	0x2000 8000	Reserved
APB bus	0x4000 0400	TMR3
APB bus	0x4000 0800	Reserved
APB bus	0x4000 1000	TMR6
APB bus	0x4000 1400	TMR7
APB bus	0x4000 1800	Reserved
APB bus	0x4000 2000	TMR14
APB bus	0x4000 2400	Reserved
APB bus	0x4000 2800	RTC
APB bus	0x4000 2C00	WWDT
APB bus	0x4000 3000	IWDT
APB bus	0x4000 3400	Reserved
APB bus	0x4000 3800	SPI2
APB bus	0x4000 3C00	Reserved
APB bus	0x4000 4400	USART2
APB bus	0x4000 4800	USART3
APB bus	0x4000 4C00	USART4
APB bus	0x4000 5000	USART5
APB bus	0x4000 5400	I2C1
APB bus	0x4000 5800	I2C2
APB bus	0x4000 5C00	Reserved
APB bus	0x4000 7000	PMU
APB bus	0x4000 7400	Reserved
—	0x4000 8000	Reserved
APB bus	0x4001 0000	SYSCFG
APB bus	0x4001 0400	EINT
APB bus	0x4001 0800	Reserved
APB bus	0x4001 1400	USART6
APB bus	0x4001 1800	Reserved
APB bus	0x4001 2400	ADC
APB bus	0x4001 2800	Reserved
APB bus	0x4001 2C00	TMR1

Region	Start address	Peripheral Name
APB bus	0x4001 3000	SPI1
APB bus	0x4001 3400	Reserved
APB bus	0x4001 3800	USART1
APB bus	0x4001 3C00	Reserved
APB bus	0x4001 4000	TMR15
APB bus	0x4001 4400	TMR16
APB bus	0x4001 4800	TMR17
APB bus	0x4001 4C00	Reserved
APB bus	0x4001 5800	DBGMCU
APB bus	0x4001 5C00	Reserved
—	0x4001 8000	Reserved
AHB1 bus	0x4002 0000	DMA
AHB1 bus	0x4002 0400	Reserved
AHB1 bus	0x4002 1000	RCM
AHB1 bus	0x4002 1400	Reserved
AHB1 bus	0x4002 2000	Flash interface
AHB1 bus	0x4002 2400	Reserved
AHB1 bus	0x4002 3000	CRC
AHB1 bus	0x4002 3400	Reserved
—	0x4002 4400	Reserved
AHB2 bus	0x4800 0000	GPIOA
AHB2 bus	0x4800 0400	GPIOB
AHB2 bus	0x4800 0800	GPIOC
AHB2 bus	0x4800 0C00	GPIOD
AHB2 bus	0x4800 1000	Reserved
AHB2 bus	0x4800 1400	GPIOF
—	0x4800 1800	Reserved
Core	0xE000 E010	STK
Core	0xE000 E100	NVIC
Core	0xE000 ED00	SCB
—	0xE010 0000	Reserved

4.1.3 Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from internal SRAM

The user can use USART interface to reprogram the user Flash if boot from BootLoader.

4.2 Core

The core of APM32F030xC is Arm® Cortex®-M0+. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3 Interrupt controller

4.3.1 Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) able to handle up to 32 maskable interrupt channels (not including 16 interrupt lines of Cortex-M0+) and 4 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 32 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 51 GPIOs can be connected to the 16 external interrupt lines.

4.4 On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program and cannot be erased.

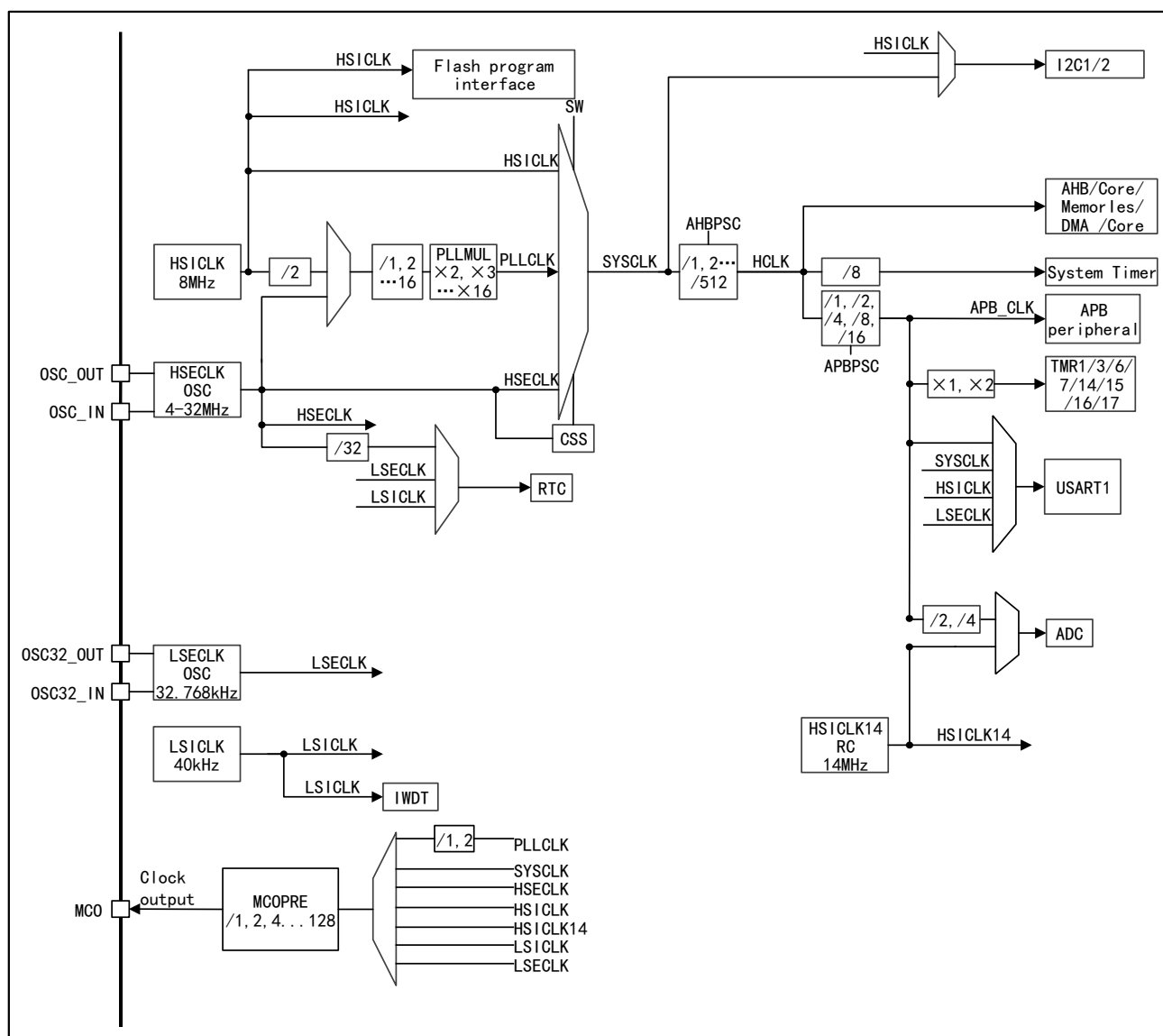
Table 10 On-chip Memory Area

Memory	Maximum capacity	Function
Main memory area	256 KB	Store user programs and data
SRAM	32 KB	CPU can access at 0 waiting cycle (read/write)
System memory area	8KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode

4.5 Clock

Clock tree of APM32F030xC is shown in the figure below:

Figure 4 APM32F030xC Clock Tree



4.5.1 Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HSI, HSE and HSI14, and the low-speed clock includes LSE and LSI; clock source is divided into internal clock and external clock according to the chip inside/outside; the internal clock includes HSI, LSI and HSI14, and the external clock includes HSE and LSE, among which HSI is calibrated by the factory to $\pm 1\%$ accuracy.

4.5.2 System clock

HSI, PLL and HSE can be selected as system clock; the clock source of PLL can be HSI or HSE; the required system clock can be obtained by configuring PLL clock multiplier factor and frequency division factor.

When the system is reset, HSI is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock by itself. When it detects

HSECLK is disabled, the system will automatically switch to the HSICLK, and if an interrupt is enabled, the software can receive the related interrupt.

4.5.3 Bus clock

AHB, APB1 and APB2 buses are built in. The clock source of AHB is SYSCLK and the clock source of APB1 and APB2 is HCLK; the required clock can be obtained by configuring the frequency division factor.

4.6 Reset and power management

4.6.1 Power supply scheme

Table 11 Power Supply Scheme

Name	Voltage range	Instruction
V_{DD}/V_{SS}	2.0~3.6V	I/Os (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V_{DD} pin.
V_{DDA}/V_{SSA}	V_{DD} ~3.6V	It supplies power to the ADC, reset module, RC oscillator and PLL analog part, and the voltage level of V_{DDA} must always be greater than or equal to the voltage level of V_{DD} , which should be provided preferentially.

4.6.2 Voltage regulator

Table 12 Regulator Operating Mode

Name	Instruction
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3 Power supply voltage monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

4.7 Low-power mode

APM32F030xC supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual application requirements.

Table 13 Low-power Mode

Mode	Instruction
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events
Stop mode	Under the condition that SRAM and register data are not lost, the stop mode can achieve the lowest power consumption; The clock of the internal 1.5V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be prohibited, and the voltage regulator can be configured in normal mode or low power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, and RTC.
Standby mode	The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.5V power supply modules are powered off, HSECLK crystal resonator, HSICLK and PLL clocks are turned off, SRAM and register data disappear, RTC area and backup register contents remain, and standby circuit still works; The external reset signal on NRST, IWDG reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

4.8 DMA

A built-in DMA, supporting 5 channels. Each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, and TMRx. Four levels of DMA channel priority can be configured. Data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" can be supported (memory includes Flash and SRAM).

4.9 GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input and output. The general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speed of 2MHz, 10MHz and 50MHz can be configured; the higher the speed is, the greater the power and the noise will be.

4.10 Communication peripherals

4.10.1 USART

Up to 6 general-purpose synchronous/asynchronous transmitter receivers are embedded in the chip, and the communication rate can support 6Mbit/s at most. All USART interfaces can be provided by DMA controller. The functions of USART interfaces are shown in the following table.

Table 14 USART Function Differences

USART mode	USART1	USART2	USART3	USART4	USART5	USART6
Hardware flow control	√	√	√	√	—	—
Multi-buffer communication (DMA)	√	√	√	√	√	√
Multi-processor communication	√	√	√	√	√	√
Synchronous	√	√	√	√	√	—
Half duplex (single-line mode)	√	√	√	√	√	√
Receiving timeout interrupt	√	√	√	—	—	—
Support the baud rate automatic detection mode	4	4	4	—	—	—

Note:

(1) "√" means this function is supported, while "—" means that this function is not supported.

4.10.2 I2C

I2C1/2 can work in master mode and slave mode, and supports 7-bit and 10-bit addressing modes. I2C1/2 supports standard mode (up to 100kbit/s) or fast mode (up to 400kbit/s). In addition, I2C1 has built-in programmable analog and digital noise filters, and also supports ultra-fast mode (up to 1 Mbit/s).

In addition, I2C1 also provides hardware support for SMBus 2.0 and PMBus 1.1: ARP function, master notification protocol, hardware CRC(PEC) generation/verification, timeout verification and alarm protocol management.

I2C supports DMA function.

4.10.3 SPI

2 built-in SPIs, support full duplex and half duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, and communicate at a rate of up to 18Mbit/s.

4.11 Analog peripherals

4.11.1 ADC

1 built-in ADC with 12-bit accuracy, up to 16 external channels and 2 internal channels for each ADC. The internal channels measure the temperature sensor voltage and reference voltage respectively. A/D conversion mode of each channel has single, continuous, scan or intermittent

modes, ADC conversion results can be left aligned or right aligned and stored in 16-bit data register; they support analog watchdog, and DMA.

4.11.1.1 Temperature sensor

A temperature sensor (TSensor) is built in, which is internally connected with ADC_IN16 channel. The voltage generated by the sensor changes linearly with temperature, and the converted voltage value can be obtained by ADC and converted into temperature.

4.11.1.2 Internal reference voltage

Built-in reference voltage V_{REFINT} , internally connected to ADC_IN17 channel, which can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC.

4.12 Timer

A built-in 16-bit advanced timer (TMR1), 5 general-purpose timers (TMR3/14/15/16/17), two basic timers (TMR6/7), an independent watchdog timer, a window watchdog timer and a system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 15 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	System tick timer	Basic timer		General-purpose timer					Advanced timer
		TMR6	TMR7	TMR3	TMR14	TMR15	TMR16	TMR17	
Timer name	Sys Tick Timer								TMR1
Counter resolution	24 bits	16 bits		16 bits					16 bits
Counter type	Down	Up		Up, down, up/down	Up	Up	Up	Up	Up, down, up/down
Prescaler factor	-	Any integer between 1 and 65536		Any integer between 1 and 65536					Any integer between 1 and 65536
General DMA request	-	OK		OK	Not OK	OK	OK	OK	OK
Capture/Comparison channel	-	-		4	1	2	1	1	4
Complementary outputs	-	-		-	-	1	1	1	3
Function Instruction	Special for real-time	Can be used as a 16-bit		Synchronization or event chaining function provided Timers in debug mode can be frozen.					It has complementary

Timer type	System tick timer	Basic timer	General-purpose timer	Advanced timer
	operating system Automatic reloading function supported When the counter is 0, it can generate a maskable system interrupt Can program the clock source	general-purpose timebase counter.	-Can be used to generate PWM output Except TMR14, each timer has independent DMA request mechanism. It can handle incremental encoder signals	PWM output with dead band insertion When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the timer can be frozen, and PWM output is disabled. Synchronization or event chaining function provided.

Table 16 Independent Watchdog and Window Watchdog Timers

Name	Counter resolution	Counter type	Prescaler factor	Functional Description
Independent watchdog	12-bit	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 40KHz, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen.

Name	Counter resolution	Counter type	Prescaler factor	Functional Description
Window watchdog	7-bit	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function; Timers in debug mode can be frozen.

4.13 RTC

A built-in RTC with LSECLK signal input pins (OSC32_IN, OSC32_OUT), 2 TAMP input signal detection pins (RTC_TAMP1/2), one reference clock input signal (RTC_REFIN), one output timestamp event output pin (RTC_TS), and one signal output pin RTC_OUT (it can be configured as calibration signal output or alarm clock signal output).

The external crystal oscillator, resonator or oscillator, LSICLK and HSECLK/32 with external frequency of 32.768kHz can be selected as the clock source.

With calendar function, it can display sub-seconds, seconds, minutes, hours (12 or 24 hours format), weeks, dates, months and years. It supports alarm clock function, and can output the alarm clock signal for external use, and wake up from low power consumption mode. It can receive signals to wake up from low power consumption mode. In terms of accuracy, it supports daylight saving time compensation, month angel compensation and leap year days compensation. In terms of precision, the error caused by crystal oscillator can be repaired by RTC digital calibration function, and the accuracy of calendar can be improved by using a more accurate second source clock (50 or 60Hz).

4.14 CRC

A CRC (cyclic redundancy check) calculation unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

5 Electrical characteristics

5.1 Test conditions of electrical characteristics

5.1.1 Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at $T_A=25^{\circ}\text{C}$. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average $\pm 3\sigma$) to get the maximum and minimum values.

5.1.2 Typical values

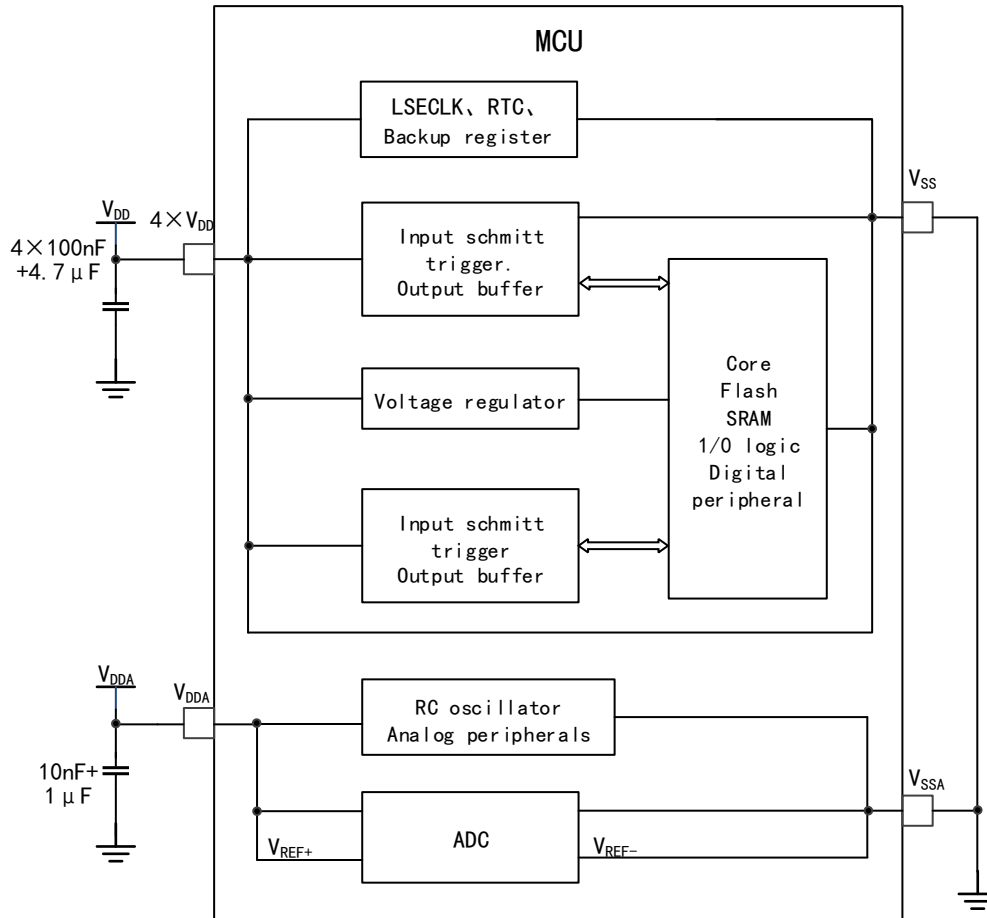
Unless otherwise specified, typical data are measured based on $T_A=25^{\circ}\text{C}$, $V_{DD}=V_{DDA}=3.3\text{V}$. these data are only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves will only be used for design guidance and will not be tested.

5.1.4 Power supply scheme

Figure 5 Power Supply Scheme



5.1.5 Load capacitance

Figure 6 Load conditions when measuring pin parameters

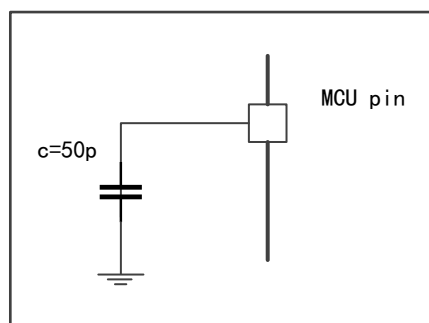


Figure 7 Pin Input Voltage Measurement Scheme

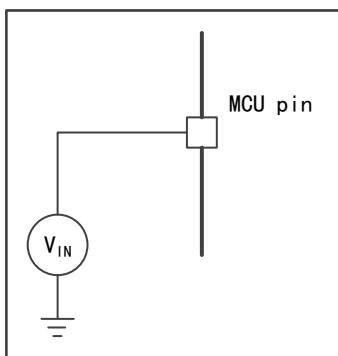
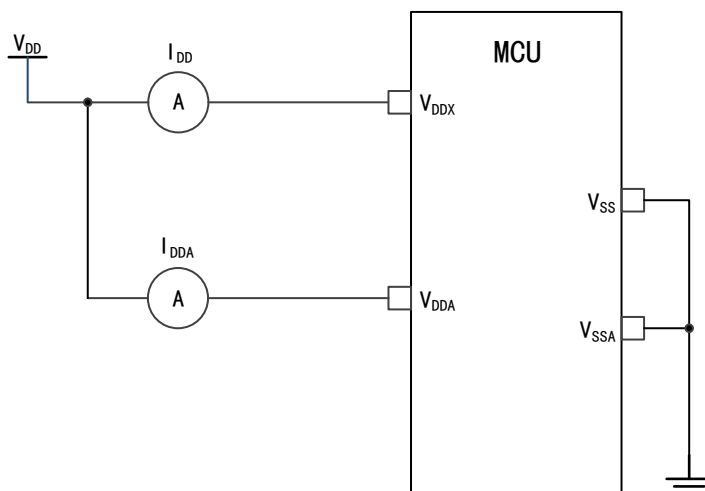


Figure 8 Power Consumption Measurement Scheme



5.2 Test under general operating conditions

Table 17 General Operating Conditions

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	48	
V_{DD}	Main power supply voltage	-	2	3.6	V
V_{DDA}	Analog power supply voltage (When ADC is not used)	Must be the same as V_{DD}	V_{DD}	3.6	V
	Analog power supply voltage (When ADC is used)		2.4	3.6	
T_A	Ambient temperature (temperature number 6)	Maximum power dissipation	-40	85	°C
	Ambient temperature (temperature number 7)	Maximum power dissipation	-40	105	°C

5.3 Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1 Maximum temperature characteristics

Table 18 Temperature Characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-55 ~ +150	°C
T_J	Maximum junction temperature	150	°C

5.3.2 Maximum rated voltage characteristics

All power supply (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 19 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
$V_{DD} - V_{SS}$	External main power supply voltage	-0.3	4.0	V
$V_{DDA} - V_{SSA}$	External analog power supply voltage	-0.3	4.0	
$V_{DD} - V_{DDA}$	Voltage difference allowed by $V_{DD} > V_{DDA}$	-	0.3	
V_{IN}	Input voltage on FT pins	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on 3.3V pin	$V_{SS} - 0.3$	4.0	
	Input voltage on other pins	$V_{SS} - 0.3$	4.0	
$ \Delta V_{DDx} $	Voltage difference between different power supply pins	-	50	mV
$ V_{SSx} - V_{SS} $	Voltage difference between different grounding pins	-	50	

5.3.3 Maximum rated current features

表格 20 Maximum Rated Current Features

Symbol	Description	Maximum	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source) ⁽¹⁾	120	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink) ⁽¹⁾	-120	
$I_{VDD (PIN)}$	Maximum current into each V_{DD} power pin (source) ⁽¹⁾	100	
$I_{VSS (PIN)}$	Maximum current out of each V_{SS} ground pin (sink) ⁽¹⁾	-100	
$I_{IO (PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	

Symbol	Description	Maximum	Unit
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	80	
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	-80	
$I_{INJ(PIN)}$ ⁽³⁾	Injected current on 5T and 5Tf pins	-5/+0 ⁽⁴⁾	
	Injected current on STD and RST pin	±5	
	Injected current on STDA pins ⁽⁵⁾	±5	
$\Sigma I_{INJ(PIN)}$	Total injection current on all I/O and control pins ⁽⁴⁾	±25	

- (1) All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
- (2) This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
- (3) A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.
- (4) Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
- (5) On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device.
- (6) When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values)

5.3.4 ESD characteristics

Table 21 ESD Characteristics

Symbol	Parameter	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25^\circ\text{C}$	6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	$T_A = +25^\circ\text{C}$	2000	

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5 Static latch-up

Table 22 Static Latch-up

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	$T_A = +25^\circ\text{C}/105^\circ\text{C}$	Class II-A

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4 On-chip memory

5.4.1 Flash characteristics

Table 23 Flash Memory Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
t _{prog}	16-bit programming time	T _A = -40~105°C V _{DD} =2.4~3.6V	-	48	-	μs
t _{ERASE}	Page (2KBytes) erase time	T _A = -40~105°C V _{DD} =2.4~3.6V	-	3	-	ms
t _{ME}	Whole erase time	T _A = 25°C V _{DD} =3.3V	-	12	-	ms
V _{prog}	Programming voltage	T _A = -40~105°C	2	-	3.6	V
t _{RET}	Data saving time	T _A =125°C	10.77	-	-	years
N _{RW}	Erase cycle	T _A =25°C	100K	-	-	cycles

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5 Clock

5.5.1 Characteristics of external clock source

High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 24 HSECLK4~32MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
f _{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R _F	Feedback resistance	-	-	300	-	kΩ
I _{DD(HSECLK)}	HSECLK current consumption	V _{DD} =3.3V, CL=10pF@8MHz	-	0.29	-	mA
t _{SU(HSECLK)}	Startup time	V _{DD} is stable	-	2	-	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 25 LSECLK Oscillator Characteristics ($f_{LSECLK}=32.768\text{KHz}$)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
f_{OSF_IN}	Oscillator frequency	-	-	32.768	-	KHz
$t_{SU(LSECLK)}^{(1)}$	Startup time	V_{DDIOx} is stable	-	2	-	s
$I_{DD(LSECLK)}$	LSECLK current consumption	-	-	0.9	-	μA

Note: It is obtained from a comprehensive evaluation and is not tested in production.

(1) $t_{SU(HXT)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.5.2 Characteristics of internal clock source

High speed internal (HSICLK) RC oscillator

Table 26 HSICLK Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit	
f_{HSICLK}	Frequency	-	-	8	-	MHz	
$A_{CCHSICLK}$	Accuracy of HSICLK oscillator	Factory calibration	$V_{DD}=3.3\text{V}$, $T_A=25^\circ\text{C}^{(1)}$	-1	-	1	%
			$V_{DD}=2\sim 3.6\text{V}$, $T_A=-40\sim 105^\circ\text{C}$	-3	-	3	%
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	$V_{DD}=3.3\text{V}$, $T_A=-40\sim 105^\circ\text{C}$	1	-	2	μs	
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-	-	80	100	μA	

Note: (1) Except for calibration in production, other data are obtained from a comprehensive evaluation and is not tested in production.

14MHz high speed internal (HSICLK14) RC oscillator

Table 27 HSICLK14 Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit	
f_{HSICLK}	Frequency	-	-	14	-	MHz	
$A_{CCHSICLK}$	Accuracy of HSICLK oscillator	Factory calibration	$V_{DD}=3.3\text{V}$, $T_A=25^\circ\text{C}^{(1)}$	-1	-	1	%
			$V_{DD}=2\sim 3.6\text{V}$, $T_A=-40\sim 105^\circ\text{C}$	-3	-	3	%

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	$V_{DD}=3.3V, T_A=-40\sim 105^{\circ}C$	1	-	2	μs
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-	-	100	150	μA

Note: (1) Except for calibration in production, other data are obtained from a comprehensive evaluation and is not tested in production.

Low speed internal (LSICLK) RC oscillator

Table 28 LSICLK Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical values	Maximum value	Unit
f_{LSICLK}	Frequency ($V_{DD}=2\sim 3.6V, T_A=-40\sim 105^{\circ}C$)	30	40	50	KHz
$t_{SU(LSICLK)}$	LSICLK oscillator startup time, ($V_{DD}=3.3V, T_A=-40\sim 105^{\circ}C$)	-	-	96	μs
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	0.75	-	μA

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.3 PLL Characteristics

Table 29 PLL Characteristics

Symbol	Parameter	Numerical Value			Unit
		Minimum value	Typical values	Maximum value	
f_{PLL_IN}	PLL input clock	1	8.0	24	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock, ($V_{DD}=3.3V, T_A=-40\sim 125^{\circ}C$)	16	-	48	MHz
t_{LOCK}	PLL phase locking time	-	-	200	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.6 Reset and power management

5.6.1 Test of Embedded Reset and Power Control Block Characteristics

Table 30 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
$V_{POR/PDR}$	Power-on/power-down	Falling edge	1.89	1.92	1.95	V

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
	reset threshold	Rising edge	1.92	1.95	1.98	V
$V_{PDRhyst}$	PDR hysteresis	-	20.00	30.00	40.00	mV
$T_{RSTTEMPO}$	Reset duration	-	1.10	1.29	1.52	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.7 Power consumption

5.7.1 Power consumption test environment

- (1) The values are measured by executing Coremark, with the Keil.V5 compilation environment and the L3 compilation optimization level.
- (2) All I/O pins are configured as analog inputs and are connected to a static level of V_{DD} or V_{SS} (non-loaded)
- (3) Unless otherwise specified, all peripherals are turned off
- (4) The relationship between Flash waiting cycle setting and f_{HCLK} :
 0~24MHz: 0 waiting cycle
 24~48MHz: 1 waiting cycle
- (5) The instruction prefetch function is enabled (Note: it must be set before clock setting and bus frequency division)
- (6) When the peripherals are enabled: $f_{PCLK} = f_{HCLK}$

5.7.2 Power consumption in run mode

Table 31 Power Consumption in Run Mode when the Program is Executed in Flash

Parameter	Conditions	f_{HCLK}	Typical value ⁽¹⁾		Maximum value ⁽¹⁾	
			$T_A=25^{\circ}C, V_{DD}=3.3V$		$T_A=105^{\circ}C, V_{DD}=3.6V$	
			$I_{DDA}(\mu A)$	$I_{DD}(mA)$	$I_{DDA}(\mu A)$	$I_{DD}(mA)$
Power consumption in run mode	HSECLK bypass ⁽²⁾ , enabling all peripherals	48MHz	103.09	14.51	116.07	15.11
		32MHz	71.88	10.05	83.44	10.50
		24MHz	58.02	7.93	69.07	8.44
		8MHz	2.17	3.17	7.35	3.64
		1MHz	2.17	1.94	7.17	2.78
	HSECLK bypass ⁽²⁾ , turning off all peripherals	48MHz	103.07	8.99	116.02	9.30
		32MHz	71.85	6.23	83.42	6.58
		24MHz	58.04	5.07	69.02	5.56
		8MHz	2.17	2.25	7.28	2.65
		1MHz	2.17	1.82	7.23	2.68

Parameter	Conditions	f _{HCLK}	Typical value ⁽¹⁾		Maximum value ⁽¹⁾	
			T _A =25°C, V _{DD} =3.3V		T _A =105°C, V _{DD} =3.6V	
			I _{DDA} (μA)	I _{DD} (mA)	I _{DDA} (μA)	I _{DD} (mA)
	HSICLK ⁽²⁾ , enabling all peripherals	48MHz	165.36	14.52	182.74	14.78
		32MHz	134.37	9.97	150.34	10.28
		24MHz	120.54	7.87	135.75	8.13
		8MHz	64.98	3.12	76.50	3.36
	HSICLK ⁽²⁾ , turning off all peripherals	48MHz	165.40	8.89	182.68	9.01
		32MHz	134.36	6.18	150.14	6.44
		24MHz	120.55	5.00	135.79	5.25
		8MHz	64.99	2.16	76.34	2.44

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 32 Power Consumption in Run Mode when the Program is Executed in RAM

Parameter	Conditions	f _{HCLK}	Typical value ⁽¹⁾		Maximum value ⁽¹⁾	
			T _A =25°C, V _{DD} =3.3V		T _A =105°C, V _{DD} =3.6V	
			I _{DDA} (μA)	I _{DD} (mA)	I _{DDA} (μA)	I _{DD} (mA)
Power consumption in run mode	HSECLK bypass ⁽²⁾ , enabling all peripherals	48MHz	103.16	12.36	12.51	12.82
		32MHz	71.93	8.52	8.77	8.74
		24MHz	58.01	6.62	6.75	6.91
		8MHz	2.17	2.70	2.89	2.93
		1MHz	2.17	0.98	1.14	1.18
	HSECLK bypass ⁽²⁾ , turning off all peripherals	48MHz	102.49	6.75	7.07	6.97
		32MHz	71.34	4.79	5.08	4.98
		24MHz	57.36	3.72	3.99	4.01
		8MHz	2.33	1.77	1.99	1.96
		1MHz	2.33	0.86	1.07	1.07
	HSICLK ⁽²⁾ , enabling all peripherals	48MHz	165.37	12.37	12.82	12.86
		32MHz	134.37	8.57	8.93	8.90
		24MHz	120.52	6.66	6.96	6.84
		8MHz	64.98	2.77	3.00	3.04
	HSICLK ⁽²⁾ , turning off all peripherals	48MHz	164.62	6.74	7.05	7.03
		32MHz	134.35	4.81	5.05	4.99

Parameter	Conditions	f _{HCLK}	Typical value ⁽¹⁾		Maximum value ⁽¹⁾	
			T _A =25°C, V _{DD} =3.3V		T _A =105°C, V _{DD} =3.6V	
			I _{DDA} (μA)	I _{DD} (mA)	I _{DDA} (μA)	I _{DD} (mA)
		24MHz	120.50	3.76	4.03	4.05
		8MHz	64.35	1.84	2.02	2.01

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

5.7.3 Power consumption in sleep mode

Table 33 Power Consumption in Sleep Mode when the Program RAM is Executed in Flash

Parameter	Conditions	f _{HCLK}	Typical value ⁽¹⁾		Maximum value ⁽¹⁾	
			T _A =25°C, V _{DD} =3.3V		T _A =105°C, V _{DD} =3.6V	
			I _{DDA} (μA)	I _{DD} (mA)	I _{DDA} (μA)	I _{DD} (mA)
Sleep mode Power consumption	HSECLK bypass ⁽²⁾ , enabling all peripherals	48MHz	103.14	9.31	116.13	9.7
		32MHz	71.93	6.52	83.37	6.96
		24MHz	58.00	5.09	69.03	5.59
		8MHz	2.17	2.25	7.23	2.65
		1MHz	2.17	1.82	7.22	1.12
	HSECLK bypass ⁽²⁾ , turning off all peripherals	48MHz	103.13	2.39	115.96	2.79
		32MHz	71.89	1.90	83.17	2.33
		24MHz	57.99	1.65	68.91	2.09
		8MHz	2.17	1.10	7.13	1.53
		1MHz	2.16	0.72	7.12	0.97
	HSICLK ⁽²⁾ , enabling all peripherals	48MHz	165.34	9.25	182.73	9.59
		32MHz	134.36	6.47	150.16	6.77
		24MHz	120.50	5.03	135.52	5.33
		8MHz	64.98	2.21	75.37	2.48
	HSICLK ⁽²⁾ , turning off all peripherals	48MHz	165.34	2.29	182.58	2.56
		32MHz	134.39	1.80	150.09	2.08
24MHz		120.51	1.55	135.39	1.82	
8MHz		64.99	1.02	75.68	1.29	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

5.7.4 Power consumption in stop mode and standby mode

Table 34 Power Consumption in Stop Mode and Standby Mode

Parameter	Conditions		Typical value ⁽¹⁾ , (T _A =25°C)						Maximum value ⁽¹⁾ , (V _{DD} =3.6V)				Unit
			V _{DD} =2.0V		V _{DD} =3.3V		V _{DD} =3.6V		T _A =85°C		T _A =105°C		
			I _D DA	I _D D	I _D DA	I _D D	I _D DA	I _D D	I _D DA	I _D D	I _D DA	I _D D	
Power consumption in stop mode	V _{DDA} Monitor ON	Regulator in run mode, all oscillators OFF	2.55	22.78	3.03	23.43	3.25	23.96	4.84	79.63	7.57	165.32	μA
		Regulator in low-power mode, all oscillators OFF	2.50	8.53	3.02	9.24	3.25	9.73	4.80	61.51	7.54	142.50	
Power consumption in standby mode		LSICLK and IWDT ON	2.70	1.72	3.40	2.62	3.70	3.18	5.21	7.18	7.65	14.37	
		LSICLK and IWDT OFF	2.37	1.43	2.90	2.25	3.13	2.69	4.66	6.66	7.11	13.88	
Power consumption in stop mode	V _{DDA} Monitor OFF	Regulator in run mode, all oscillators OFF	1.35	22.73	1.53	23.62	1.64	24.05	3.16	79.76	5.95	165.3	
		Regulator in low-power mode, all oscillators OFF	1.35	8.50	1.52	9.35	1.63	9.77	3.14	61.66	5.88	143.7	
Power consumption in standby mode		LSICLK and IWDT ON	1.55	1.71	1.90	2.75	2.06	3.23	3.54	7.23	6.01	14.46	
		LSICLK and IWDT OFF	1.22	1.42	1.40	2.30	1.51	2.74	2.99	6.74	5.46	13.89	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.5 Peripheral power consumption

The HSECLK Bypass 1M is adopted as clock source, $f_{PCLK}=f_{HCLK}=1M$.

Peripheral power consumption = current that enables the peripheral clock-current that disables the peripheral clock.

Table 35 Peripheral Power Consumption

Parameter	Peripheral	Typical value ⁽¹⁾ T _A =25°C, V _{DD} =3.3V	Unit
Peripheral power consumption	BusMatrix	1.12	μA/MHz
	CRC	0.70	
	DMA	2.25	
	FLASH	23.75	
	GPIOA	2.25	
	GPIOB	2.12	
	GPIOC	0.87	
	GIOD	0.79	
	GPIOF	0.71	
	SRAM	0.25	
	ALL_AHB	41.04	
	APB_Bridge	1.00	
	ADC	3.00	
	CAN	6.62	
	DAC	2.46	
	DBGMCU	0.25	
	I2C1	7.54	
	I2C2	1.87	
	PMU	0.91	
	SPI1	4.91	
	SPI2	4.5	
	SYSCFG	1.08	
	TMR1	6.95	
	TMR3	5.20	
TMR6	1.41		
TMR7	1.33		
TMR14	2.70		

Parameter	Peripheral	Typical value ⁽¹⁾ T _A =25°C, V _{DD} =3.3V	Unit
	TMR15	4.20	
	TMR16	3.20	
	TMR17	3.58	
	USART1	9.08	
	USART2	9.10	
	USART3	9.04	
	USART4	3.2	
	ALL_APB	114.62	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.8 Wake-up time in low power mode

The measurement of wake-up time in low power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 36 Wake Up Time in Low-power Mode

Symbol	Parameter	Conditions	Typical value (T _A =25°C)			Maximum value	Unit
			2V	3.3V	3.6V		
t _{WUSLEEP}	Wake-up from sleep mode	-	0.15	0.15	0.15	0.17	μs
t _{WUSTOP}	Wake up from stop mode	The voltage regulator is in run mode	3.45	3.09	3.02	3.89	
		The voltage regulator is in low power mode	8.15	5.43	5.14	9.72	
t _{WUSTDBY}	Wake up from standby mode	-	46.65	37.15	35.93	53.80	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.9 Pin characteristics

5.9.1 I/O pin characteristics

Table 37 DC Characteristics (test condition of V_{DD} =2.7~3.6V, T_A =-40~105°C)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V _{IL}	Low level input voltage	STD and STDA I/O	-	-	0.3V _{DDIOx} +0.07	V
		5T and 5Tf I/O	-	-	0.475V _{DDIOx} -0.2	
		I/O pins except Boot0 pin	-	-	0.3V _{DDIOx}	

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V_{IH}	High level input voltage	STD and STDA I/O	$0.445V_{DDIOx} + 0.398$	-	-	V
		5T and 5Tf I/O	$0.5V_{DDIOx} + 0.2$	-	-	
		I/O pins except Boot0 pin	$0.7V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	STD and STDA I/O	-	300	-	mV
		5T and 5Tf I/O	-	300	-	
I_{ikg}	Input leakage current	STD, 5T and 5Tf I/OTTA in digital mode, $V_{SS} \leq V_{IN} \leq V_{DDIOx}$	-	-	+0.1	μA
		STDA in digital mode, $V_{DDIOx} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		5T and 5Tf I/O $V_{DDIOx} \leq V_{IN} \leq 5V$	-	-	10	
R_{PU}	Weak pull-up equivalent resistance	$V_{IN} = V_{SS}$	22	42	46	k Ω
R_{PD}	Weak pull-down equivalent resistance	$V_{IN} = V_{DDIOx}$	22	42	46	k Ω

Note: It is obtained from a comprehensive evaluation and is not tested in production.

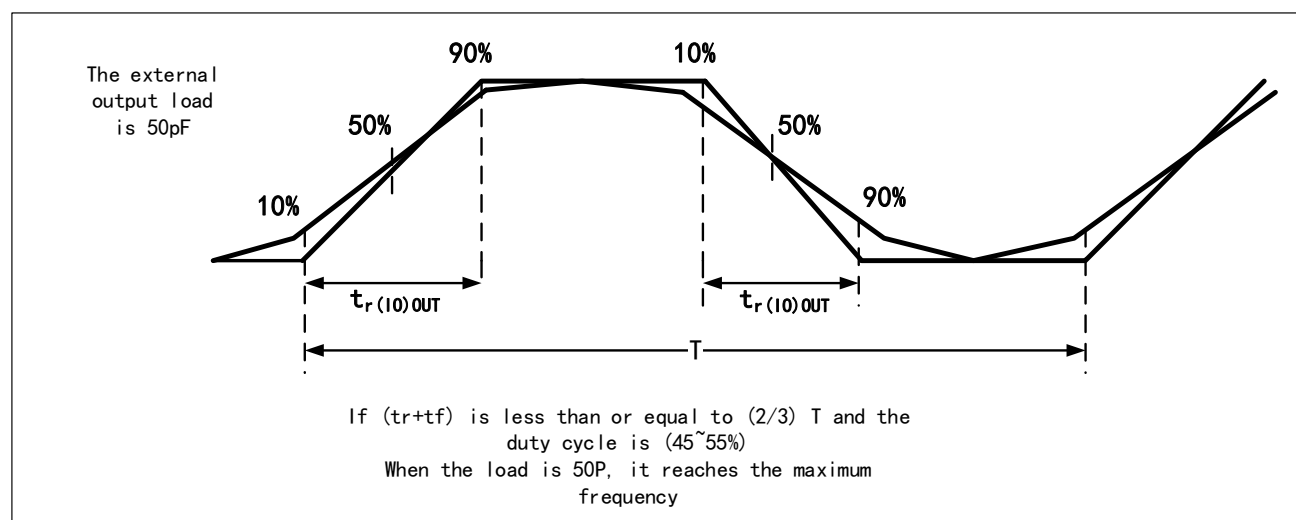
Table 38 AC Characteristics ($T_A = 25^\circ C$)

OSSELY[1:0]	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
X0(2MHz)	$f_{max(IO)out}$	Maximum frequency	$C_L = 50pF,$ $V_{DDIOx} = 2 \sim 3.6V$	-	2	MHz
	$t_{f(IO)out}$	Output fall time from high to low level		-	18.16	
	$t_{r(IO)out}$	Output rise time from low to high level		-	16.66	ns
01(10MHz)	$f_{max(IO)out}$	Maximum frequency	$C_L = 50pF,$ $V_{DDIOx} = 2 \sim 3.6V$	-	10	MHz
	$t_{f(IO)out}$	Output fall time from high to low level		-	11.50	
	$t_{r(IO)out}$	Output rise time from low to high level		-	11.14	ns
10(50MHz)	$f_{max(IO)out}$	Maximum frequency	$C_L = 30pF,$ $V_{DD} = 2.7 \sim 3.6V$	-	50	MHz
	$t_{f(IO)out}$	Output fall time from high to low level		-	3.58	

OSSELy[1:0]	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
	$t_{r(I/O)out}$	Output rise time from low to high level		-	8.06	
FM+ configuration	$f_{max(I/O)out}$	Maximum frequency	$C_L=50pF,$ $V_{DDIOx} \geq 2V$	-	2	MHz
	$t_{f(I/O)out}$	Output fall time		-	11	ns
	$t_{r(I/O)out}$	Output rise time		-	33	
FM+ configuration	$f_{max(I/O)out}$	Maximum frequency	$C_L=50pF,$ $V_{DDIOx} < 2V$	-	0.5	MHz
	$t_{f(I/O)out}$	Output fall time		-	14	ns
	$t_{r(I/O)out}$	Output rise time		-	43	

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

Figure 9 I/O AC Characteristics Definition



Note: It is obtained from a comprehensive evaluation and is not tested in production.

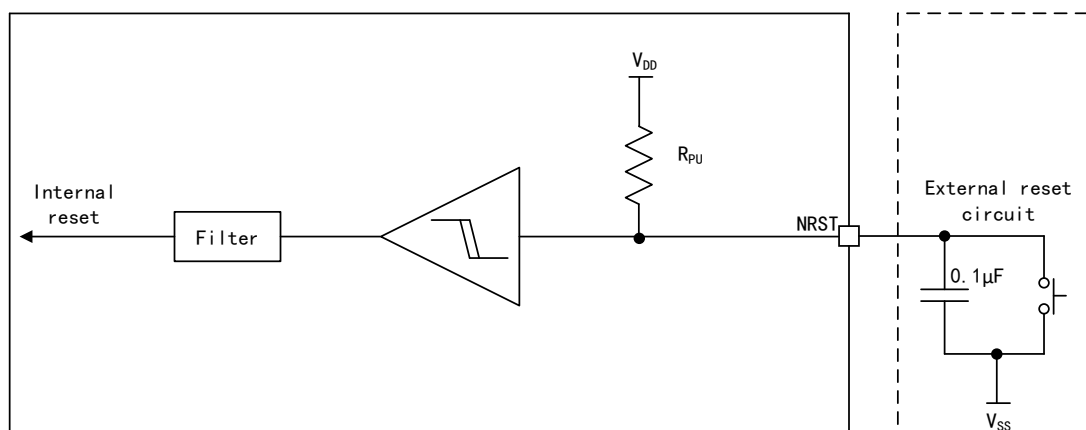
Table 39 Output Drive Current Characteristics ($T_A = 25^\circ C$)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V_{OL}	I/O pin outputs low voltage	$ I_{IO} =8mA,$ $V_{DDIOx} \geq 2.7V$	-	0.4	V
V_{OH}	I/O pin outputs high voltage		$V_{DDIOx}-0.4$	-	
V_{OL}	I/O pin outputs low voltage	$ I_{IO} =20mA,$ $V_{DDIOx} \geq 2.7V$	-	1.3	
V_{OH}	I/O pin outputs high voltage		$V_{DDIOx}-1.3$	-	

5.9.2 NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU} .

Figure 10 Recommended NRST pin protection scheme



Note:

- (1) If resetting the device, it is necessary to ensure that the NRST pin level voltage is below the maximum value of $V_{IL(NRST)}$.
- (2) The device is protected by external reset circuit capacitors and is not affected by parasitic reset.

Table 40 NRST Pin Characteristics (test condition of $V_{DD} = 2.7 \sim 3.6V$, $T_A = -40 \sim 105^\circ C$)

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
$V_{IL(NRST)}$	NRST low level input voltage	-	1.44	1.75	1.8	V
$V_{IH(NRST)}$	NRST high level input voltage	-	0	1.37	1.38	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	-0.38	-	V
R_{PU}	Weak pull-up equivalent resistance	$V_{IN} = V_{SS}$	25	40	55	k Ω

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.10 Communication peripherals

5.10.1 I2C peripheral characteristics

- Standard mode (Sm): Up to 100kbit/s
- Fast mode (Fm): Up to 400 kbit/s
- Ultra fast mode (Fm+): Up to 1 Mbit/s

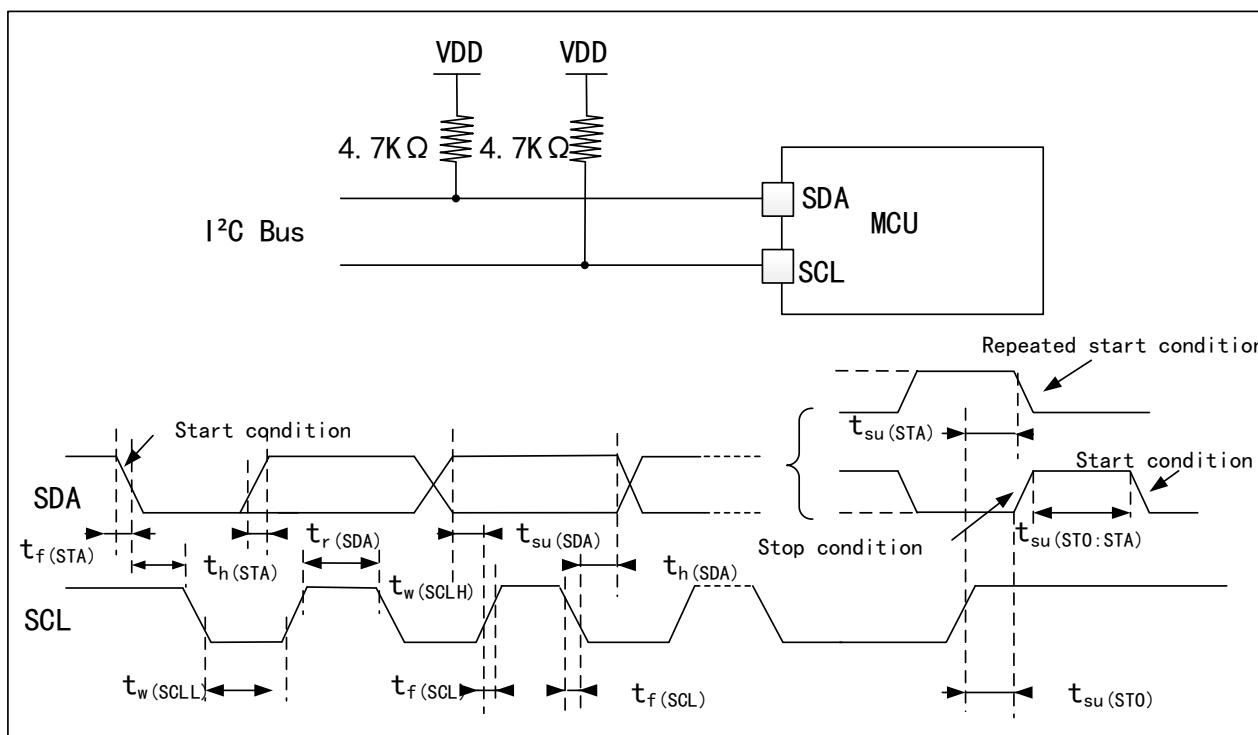
Table 41 I2C Characteristics ($T_A = 25^\circ C$, $V_{DD} = 3.3V$)

Symbol	Parameter	Standard I2C		Fast I2C		Ultra fast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(SCL)}$	SCL clock low time	4.82	-	1.67	-	0.54	-	μs

Symbol	Parameter	Standard I2C		Fast I2C		Ultra fast I2C		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(SCLH)}$	SCL clock high time	5.09	-	0.80	-	0.45	-	ns
$t_{su(SDA)}$	SDA setup time	4570	-	1432	-	311.11	-	
$t_h(SDA)$	SDA data hold time	0	176.75	0	156.17	0	150.86	
$t_r(SDA)/t_r(SCL)$	SDA and SCL rise time	-	310.05	-	301.37	-	314.08	
$t_f(SDA)/t_f(SCL)$	SDA and SCL fall time	-	3.05	-	3.61	-	5.19	
$t_h(STA)$	Start condition hold time	5.00	-	0.69	-	0.35	-	μs
$t_{su(STA)}$	Repeated start condition setup time	5.19	-	0.91	-	0.56	-	
$t_{su(STO)}$	Setup time of stop condition	4.91	-	1.78	-	0.66	-	
$t_w(STO:STA)$	Time from stop condition to start condition (bus idle)	6.46	-	6.31	-	5.80	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 11 Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.10.2 SPI peripheral characteristics

Table 42 SPI Characteristics ($T_A=25^{\circ}\text{C}$, $V_{DD}=3.3\text{V}$)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{SCK} $1/t_{\text{c(SCK)}}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{\text{r(SCK)}}$ $t_{\text{f(SCK)}}$	SI clock rise and fall time	Load capacitance: $C = 30\text{pF}$	-	6.0	ns
$t_{\text{su(NSS)}}$	NSS setup time	Slave mode	109.46	-	ns
$t_{\text{h(NSS)}}$	NSS hold time	Slave mode	81.41	-	ns
$t_{\text{w(SCKH)}}$ $t_{\text{w(SCKL)}}$	SCK high and low time	Main mode, $f_{\text{PCLK}} = 36\text{MHz}$, Prescaler factor=4	49	50	ns
$t_{\text{su(MI)}}$ $t_{\text{su(SI)}}$	Data input setup time	Master mode	15.40	-	ns
		Slave mode	23.50	-	
$t_{\text{h(MI)}}$ $t_{\text{h(SI)}}$	Data input hold time	Master mode	32.74	-	ns
		Slave mode	26.71	-	
$t_{\text{a(SO)}}$	Data output access time	Slave mode, $f_{\text{PCLK}} = 20\text{MHz}$	8.05	10.66	ns
$t_{\text{dis(SO)}}$	Data output prohibition time	Slave mode	5.67	-	ns
$t_{\text{v(SO)}}$	Effective time of data output	Slave mode (after enable edge)	-	13.48	ns
$t_{\text{v(MO)}}$	Effective time of data output	Master mode (after enable edge)	-	5.81	ns
$t_{\text{h(SO)}}$	Data output hold time	Slave mode (after enable edge)	8.83	-	ns
$t_{\text{h(MO)}}$		Master mode (after enable edge)	1.63	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 12 SPI Timing Diagram - Slave Mode and CPHA=0

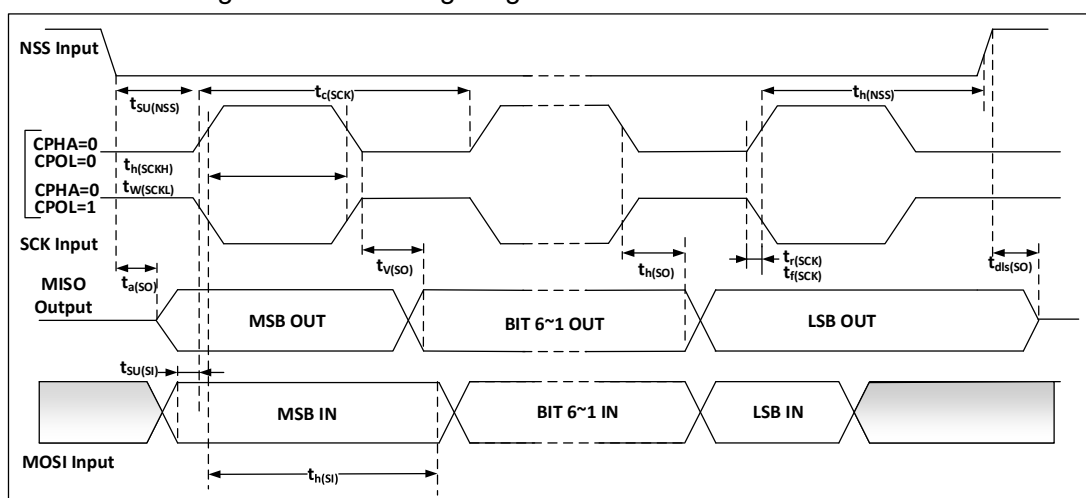
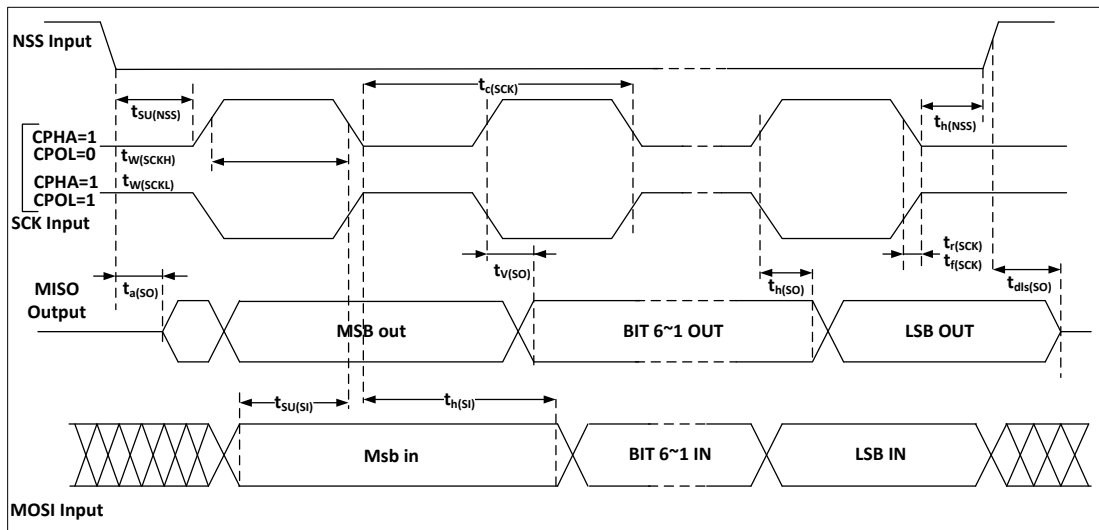
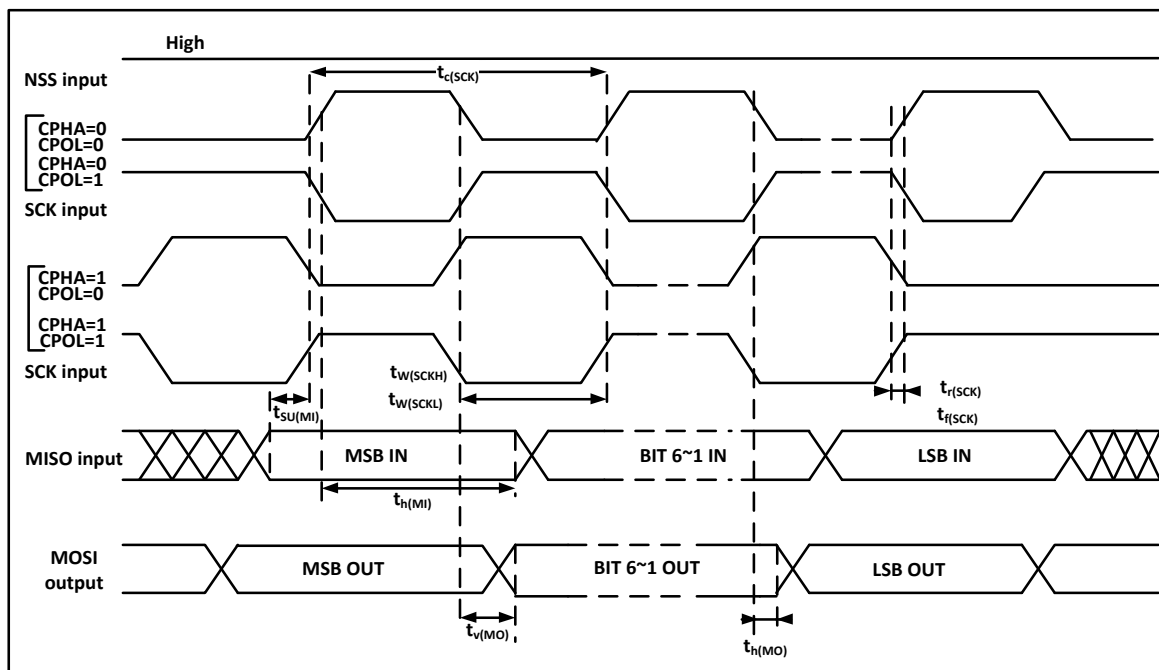


Figure 13 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: 0.3V_{DD} and 0.7V_{DD} .

Figure 14 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: 0.3V_{DD} and 0.7V_{DD} .

5.11 Analog peripherals

5.11.1 ADC

Test parameter description:

- Sampling rate: the number of conversion of analog quantity to digital quantity by ADC per second
Sample rate=ADC clock/(number of sampling periods + number of conversion periods)

5.11.1.1 12-bit ADC characteristics

Table 43 12-bit ADC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V _{DDA}	Power supply voltage	-	2.4	-	3.6	V
I _{DDA}	ADC power consumption	V _{DDA} =3.3V, f _{ADC} =14MHz, Sampling time=1.5 f _{ADC}	-	1	-	mA
f _{ADC}	ADC frequency	-	0.6	-	14	MHz
C _{ADC}	Internal sampling and holding capacitance	-	-	8	-	pF
R _{ADC}	Sampling resistor	-	-	-	1000	Ω
t _s	Sample Time	f _{ADC} =14MHz	0.107	-	17.1	μs
T _{CONV}	Sampling and conversion time	f _{ADC} =14MHz, 12-bit conversion	1	-	18	μs

Table 44 12-bit ADC Accuracy

Symbol	Parameter	Conditions	Typical values	Maximum value	Unit
ET	Composite error	f _{PCLK} =48M, f _{ADC} =12M, V _{DDA} =2.4V-3.6V T _A =-40°C~105°C	-	3.8	LSB
EO	Offset error		-	2.7	
EG	Gain error		-	1.9	
ED	Differential linear error		-	1	
EL	Integral linear error		-	3.4	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.1.2 Test of Built-in Reference Voltage Characteristics

Table 45 Embedded Reference Voltage Characteristics

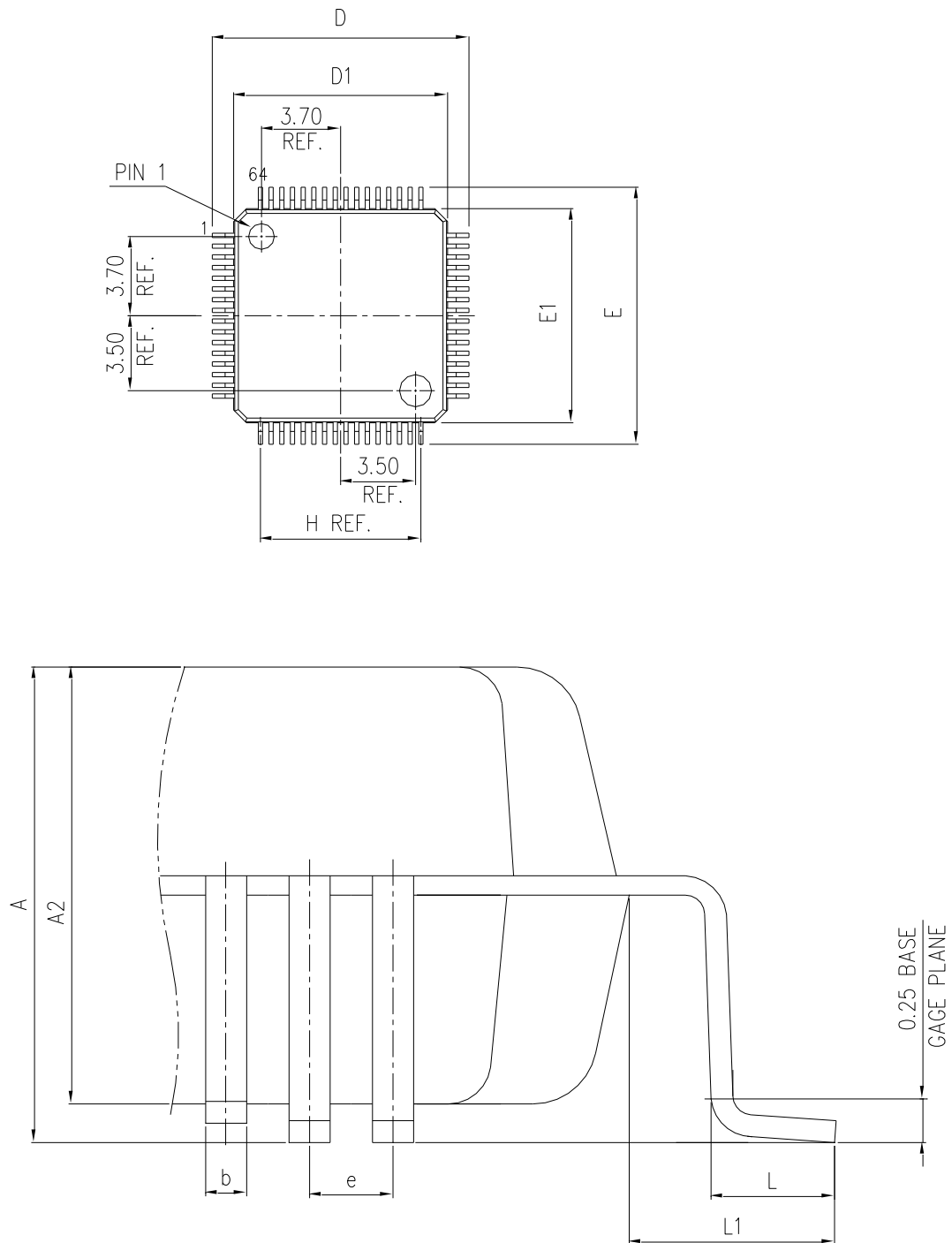
Symbol	Parameter	Conditions	Minimum value	Typical values	Maximum value	Unit
V _{REFINT}	Built-in Reference Voltage	-40°C < T _A < +105°C V _{DD} = 2-3.6V	1.19	1.23	1.27	V
t _{START}	ADC_IN17 buffer startup time	-	-	-	10	μs
T _{S_} _{refint}	Sampling time of ADC when reading out internal reference voltage	-	4	-	-	μs
ΔV _{REFINT}	Built-in reference voltage extends to temperature range	V _{DDA} =3.3V	-	-	25	mV

Note: It is obtained from a comprehensive evaluation and is not tested in production.

6 Package information

6.1 LQFP64 Package Diagram

Figure 15 LQFP64 Package Diagram



- (1) The figure is not drawn to scale.
- (2) All pins should be soldered to the PCB

Table 46 LQFP64 Package Data

DIMENSION LIST (FOOTPRINT: 2.00)			
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	12.000±0.200	LEAD TIP TO TIP
4	D1	10.000±0.100	PKG LENGTH
5	E	12.000±0.200	LEAD TIP TO TIP
6	E1	10.000±0.100	PKG WPTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H (REF)	(7.500)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

(1) Dimensions are expressed in mm

Figure 16 LQFP64-64 pins, 10×10mm recommended welding Layout

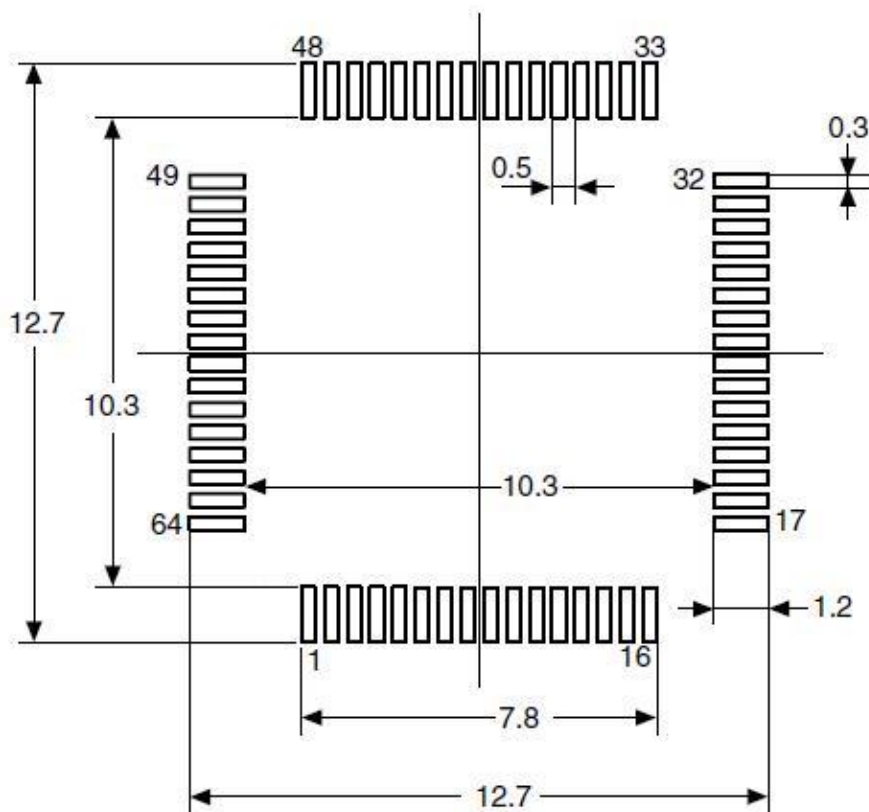
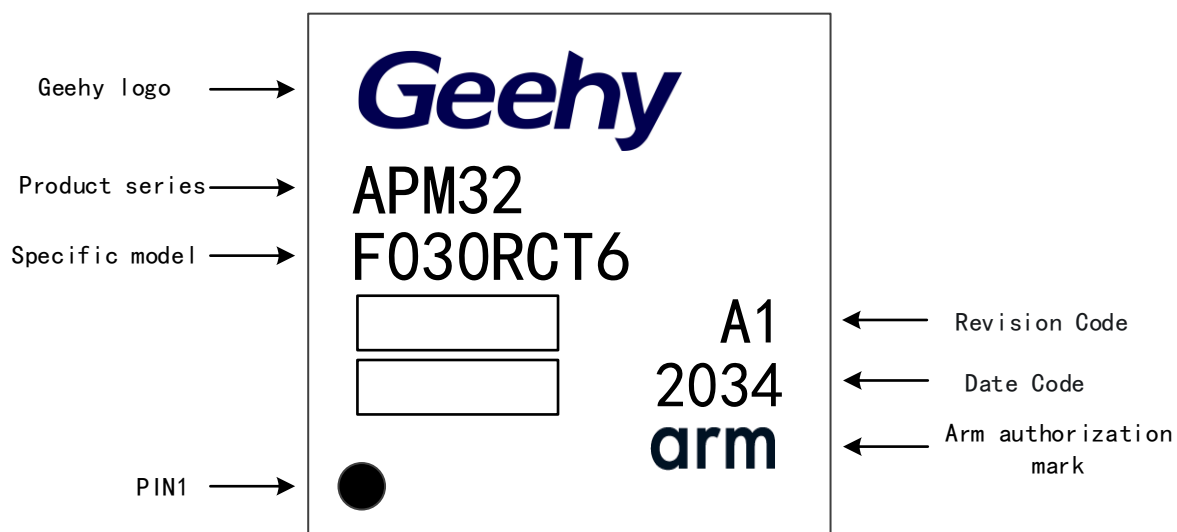
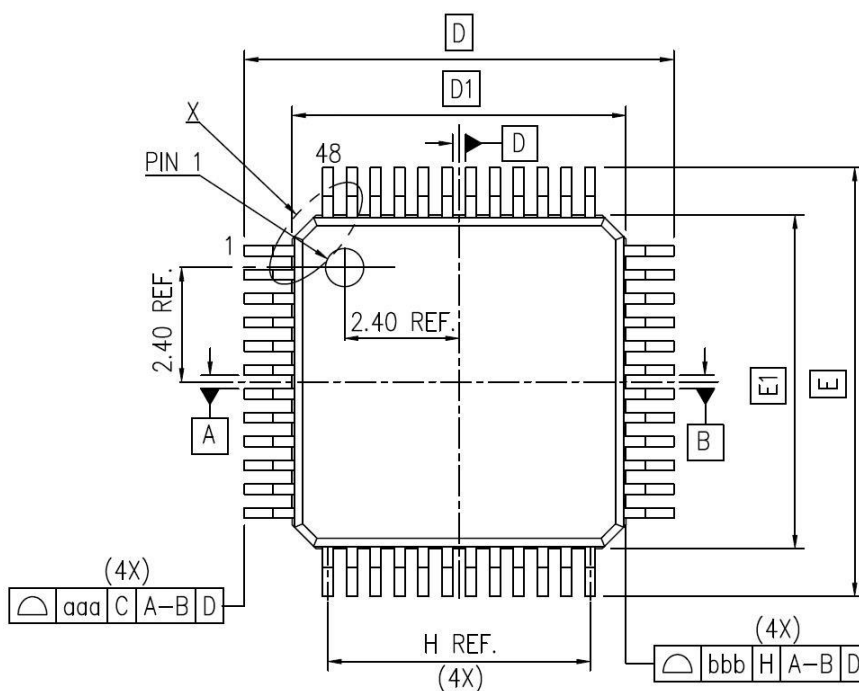


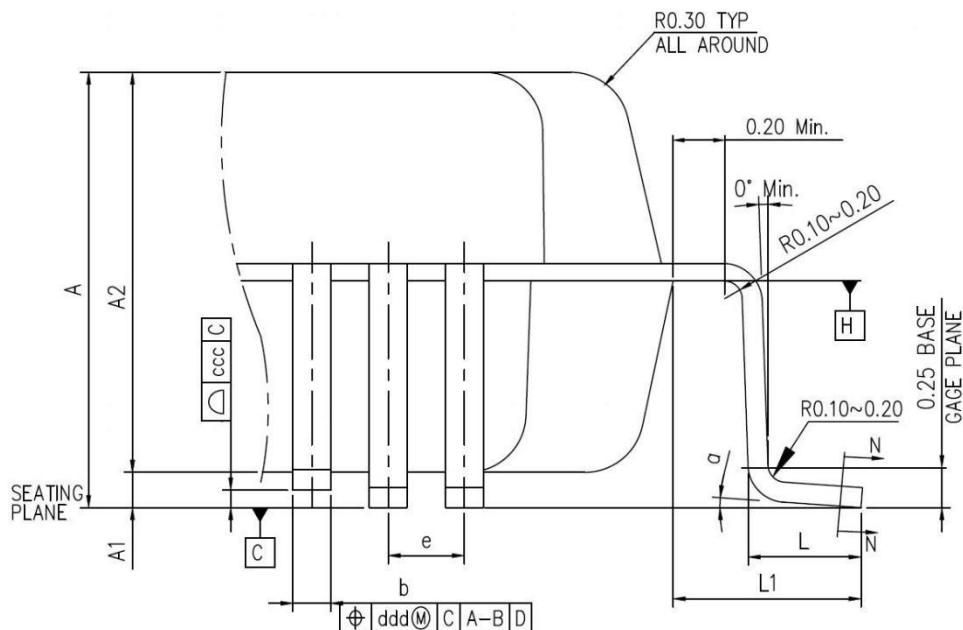
Figure 17 LQFP64-64 pins, 10×10mm package identification



6.2 LQFP48 Package Diagram

Figure 18 LQFP48 Package Diagram





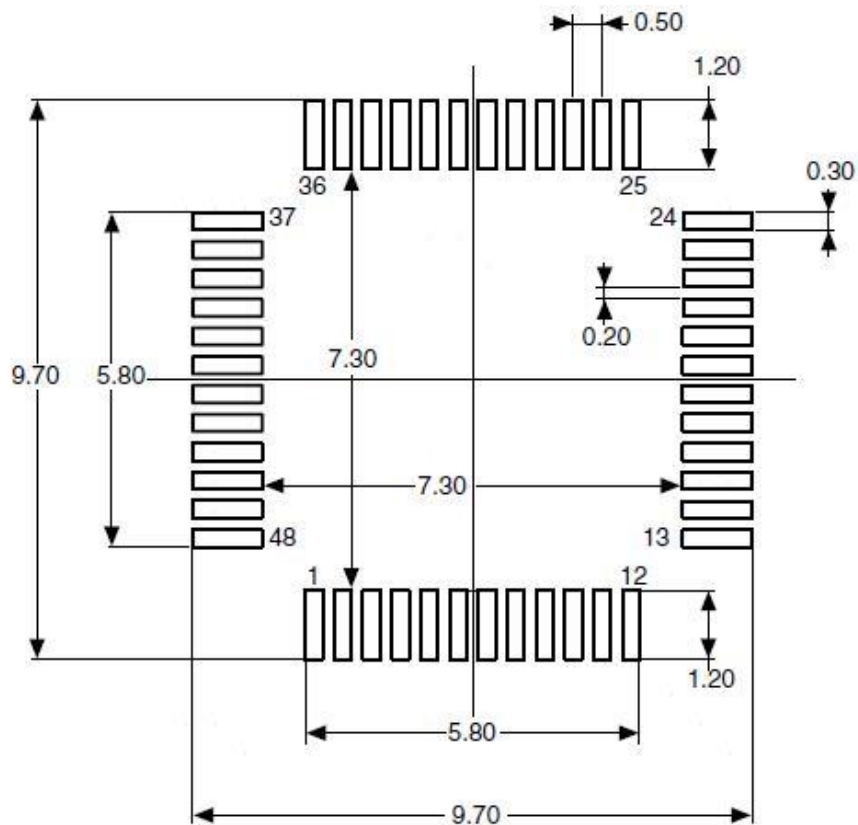
- (1) The figure is not drawn to scale.
- (2) All pins should be soldered to the PCB

Table 47 LQFP48 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)			
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.1±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	9.00±0.20	LEAD TIP TO TIP
5	D1	7.00±0.10	PKG LENGTH
6	E	9.00±0.20	LEAD TIP TO TIP
7	E1	7.00±0.10	PKG WIDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF	LEAD LENGTH
10	T	0.15	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.02	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(5.50)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

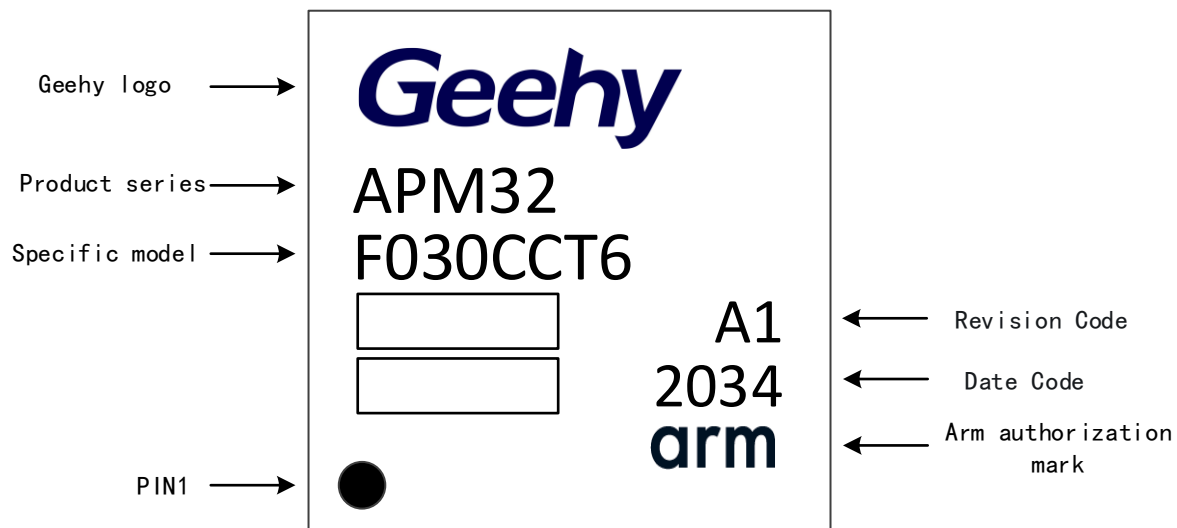
- (1) Dimensions are expressed in mm

Figure 19 LQFP48, 7×7mm Recommended Welding Layout



(1) Dimensions are expressed in mm

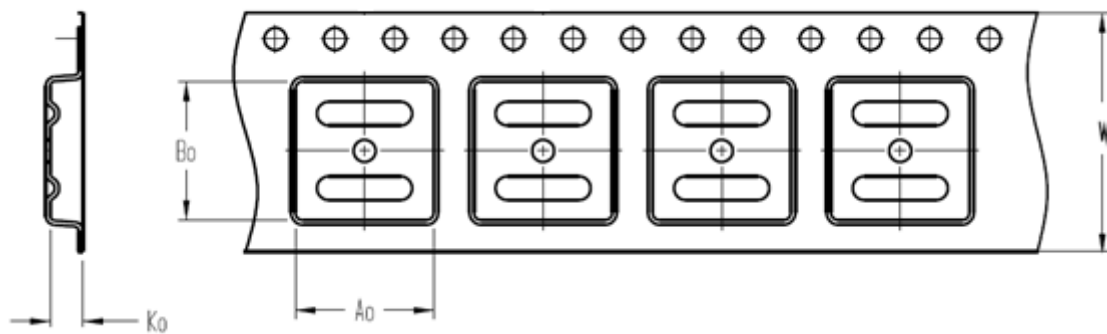
Figure 20 LQFP48-48 pins, 7×7mm identification diagram



7 Packaging Information

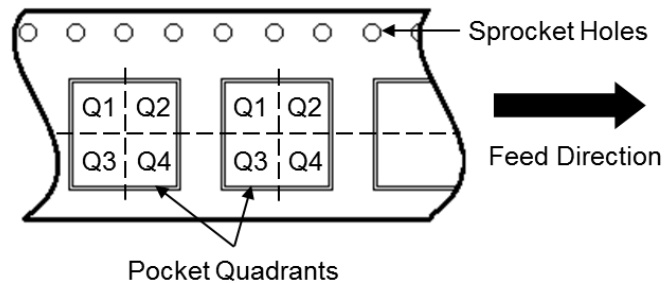
7.1 Reel Packaging

Figure 21 Specification Drawing of Reel Packaging

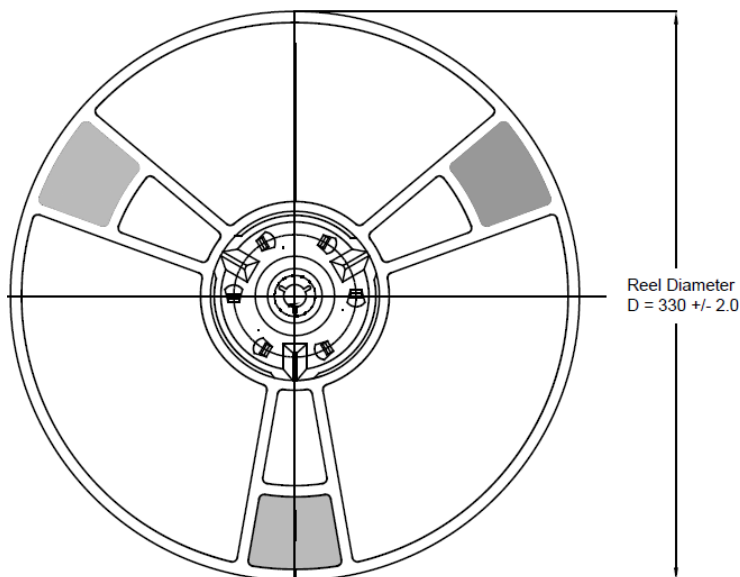


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



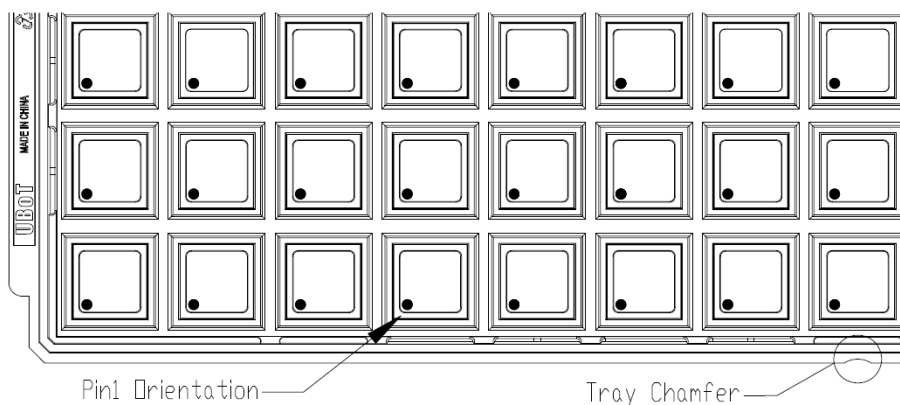
All photos are for reference only, and the appearance is subject to the product.

Table 48 Reel Packaging Parameter Specification Table

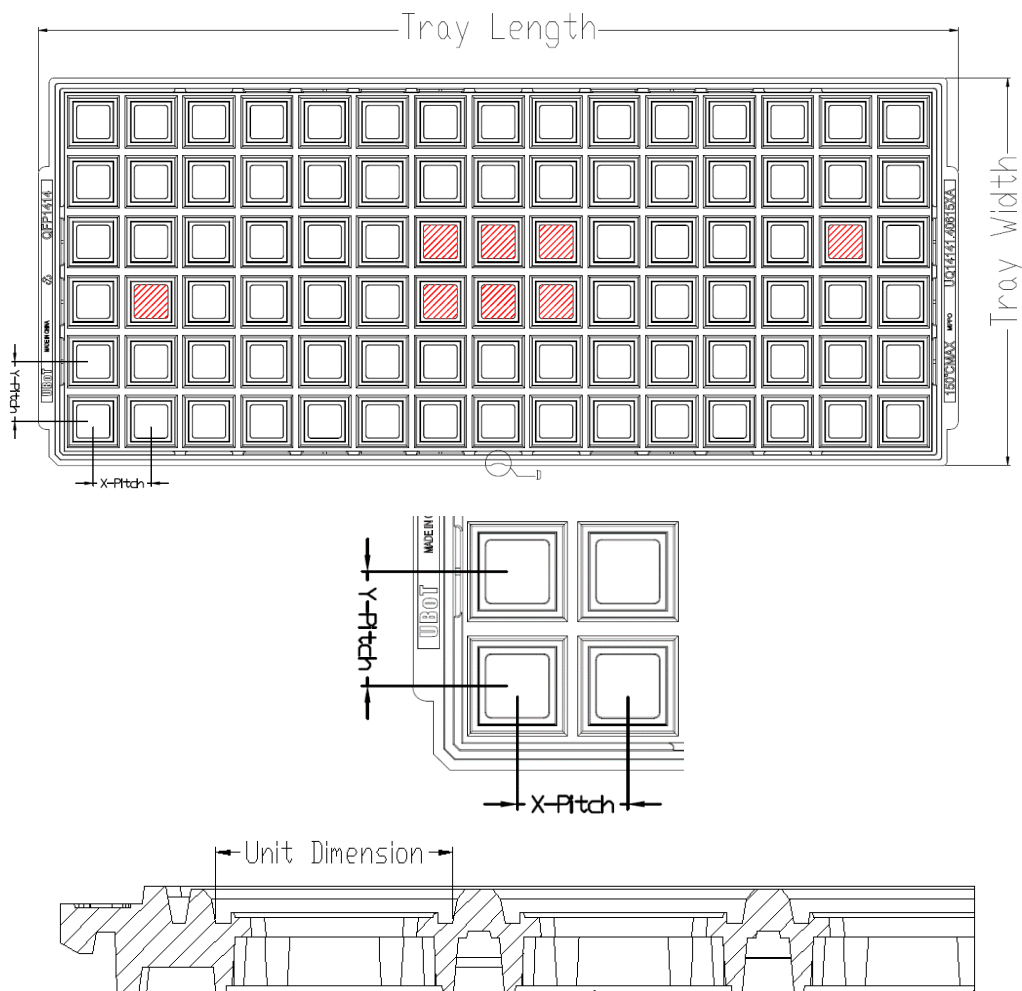
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32F030RCT6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F030CCT6	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
APM32F030RCT7	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F030CCT7	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1

7.2 Tray packaging

Figure 22 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product.

Table 49 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32F030RCT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F030CCT6	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
APM32F030RCT7	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F030CCT7	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9

8 Ordering Information

Figure 23 Product Naming Rules

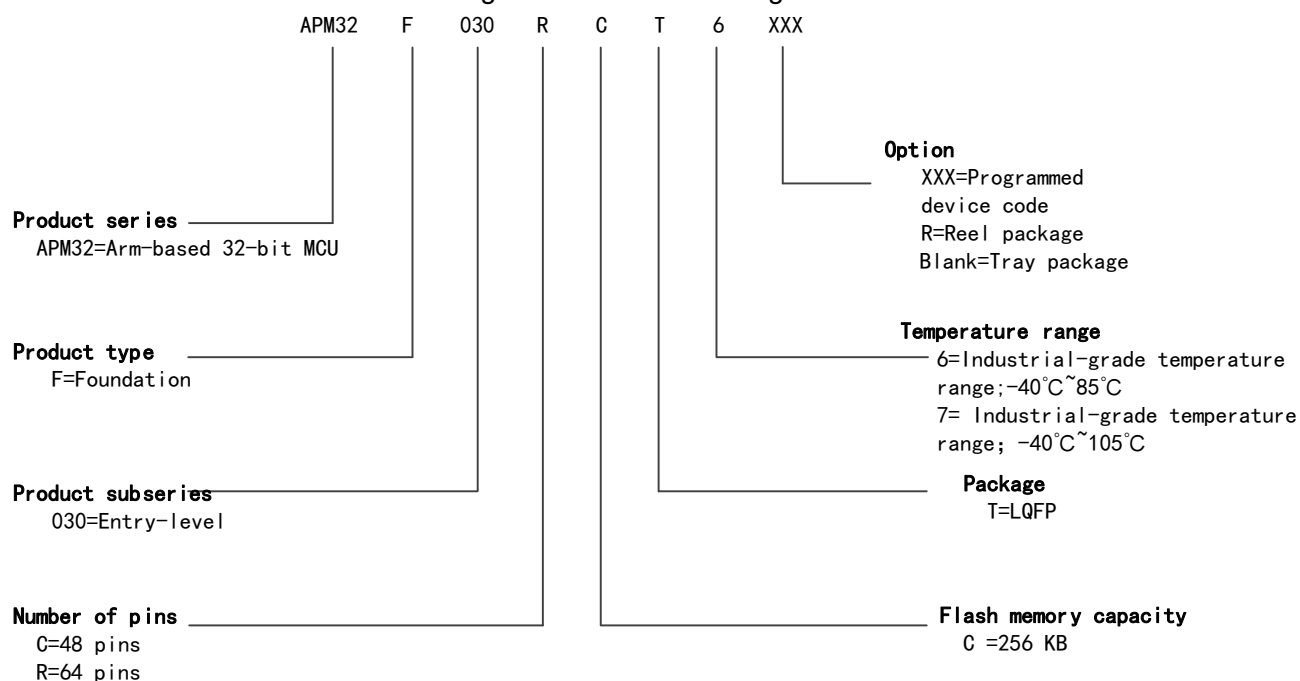


Table 50 Ordering Information Table

Order Code	Flash (KB)	SRAM (KB)	Package	SPQ	Temperature Range
APM32F030CCT6-R	256	32	LQFP48	2000	Industrial grade -40°C~85°C
APM32F030CCT6	256	32	LQFP48	2500	Industrial grade -40°C~85°C
APM32F030RCT6-R	256	32	LQFP64	1000	Industrial grade -40°C~85°C
APM32F030RCT6	256	32	LQFP64	1600	Industrial grade -40°C~85°C
APM32F030CCT7-R	256	32	LQFP48	2000	Industrial grade -40°C~105°C
APM32F030CCT7	256	32	LQFP48	2500	Industrial grade -40°C~105°C
APM32F030RCT7-R	256	32	LQFP64	1000	Industrial grade -40°C~105°C
APM32F030RCT7	256	32	LQFP64	1600	Industrial grade -40°C~105°C

Note :SPQ= Smallest Packaging Quantity

9 Commonly Used Function Module Denomination

Table 51 Commonly Used Function Module Denomination

Full name	Short name
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External interrupt	EINT
Genera-purpose IO	GPIO
Alternate function IO	AFIO
Wake up controller	WUPT
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller local area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC

10 Version History

Table 52 Document Version History

Date	Version	Change History
March 10, 2021	1.0	New
June 30 2021	1.1	Add Maximum Rated Current Features
June 22 2022	1.2	(1) Modify Arm trademark (2) Add the statement (3) Modify product naming rules figure
August 25, 2022	1.3	Change the power consumption in standby mode
March 8, 2023	1.4	(1) Modify the Function Comparison between Advanced/General-purpose/Basic and System Tick Timers table
October, 2024	1.5	(1) Design requirements for supplementary reset pins (2) Increase flash storage time and erase cycle

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